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Scatterometry solutions for 14nm half-pitch BEOL layers patterned by EUV single exposure

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ABSTRACT

To keep up with logic area scaling, BEOL dimensions have been reduced at an accelerated pace, leading to ever smaller metal pitches and reduced cross-sectional areas of the wires. As a result, routing congestion and a dramatic RC delay (resulting from an increased resistance-capacitance (RC) product) have become important bottlenecks for further interconnect scaling, driving the need for introducing new materials and integration schemes in the BEOL.

The current paper studies the damascene process flow that uses a single exposure EUV to create metal lines and 2D patterns at metal half-pitch of 14nm, corresponding to the imec N5 node for logic BEOL layer. A bright field mask with a negative tone resist process was used to develop trenches and transfer these patterns into an oxide dielectric layer. Following this, the trenches were filled with ruthenium (Ru) for electrically testing. Test vehicle included multiple structures, including E-test resistance and capacitance structures, to allow a comprehensive study of the proposed process flow.

Metrology requirements and performance at various process steps will be discussed in this paper. Our focus will be on the scatterometry methods that together with machine learning (ML) allow fast and accurate measurements of multiple parameters of interest at large sampling. In the current paper, we present results for inline measurements of line and space critical dimensions (CD), line edge roughness (LER) – after patterning and after hard mask etch, and the prediction of the electrical performance of the metal lines after Ru CMP. In addition, scatterometry ML capabilities for inline tip-to-tip (T2T) measurements are successfully demonstrated.

Keywords: EUV lithography, bright field EUV mask, pitch 28m, scatterometry, Ruthenium damascene metallization, machine learning, process control, E-test prediction, resistance, and capacitance

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1. INTRODUCTION

The integrated circuit (IC) manufacturers are well known for their drive to continuously shrink device features, increasing drive current, and reducing voltage. This drive has often resulted in the complex 3D architecture of devices and increased the relative importance of metrology [1]. The role of metrology in IC manufacturing includes exploratory research, technology development, as well as process control. Techniques like scatterometry and CDSEM are typically used for inline CD measurements. However, each method has its limitations and advantages. For instance, uncertainty in material properties (n&k) and long model-optimization times restrict scatterometry techniques, while resist shrinkage and its charging effect impact the SEM tool's measurement performance [2].

Scatterometry has been established as a fast, non-destructive metrology method providing complete profile information of fins in FEOL and the interconnect lines in BEOL [3]. Figure 1 shows a schematic explaining the operation of the scatterometry tool. Traditional scatterometry model building needs a longer time to solution, especially in R&D. Modelling of non-periodic structures can be problematic and can take even longer. Moreover, strict process control budgets may be compromised by model errors. For these reasons, direct measurements of all the essential parameters may not be possible, which leads to the need for predictive statistical approaches [4].

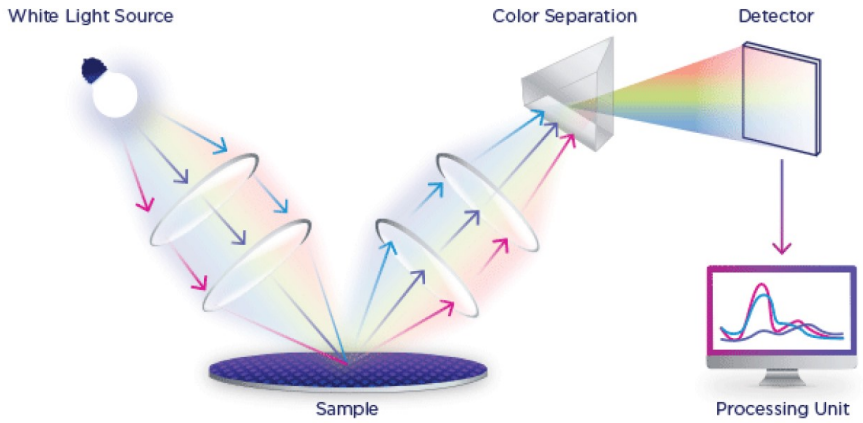

Figure 1 Schematic of scatterometry spectra collection and data analysis

Machine learning (ML) solutions have become an attractive tool for process control and monitoring purposes and E-test prediction [3,5,6]. The methodology involves cross combining the inline scatterometry spectra with reference data. Then, a mathematical estimator is generated using a set of ML algorithms. The data used to create the mathematical estimator is the training set. Once the training is completed and shows a good correlation to the reference data, the scatterometry spectra are used to measure and predict parameters of interest on other wafers. ML capabilities were successfully demonstrated for inline CDs [7] and EOL E-test resistance for HVM production [3].

Additionally, the ML technique is less dependent on the measured patterns' structural complexity and can also measure on the non-periodic targets. The model optimization is done by the design of

experiment (DOE) methodology. Extreme process window corners can be used during training the data set to ensure ML can measure all process variations.

ML-based inline scatterometry measurements allow early awareness of the electrical performance and variability and significantly reduce costs for both R&D and high-volume manufacturing (HVM) by taking the proper action on time to either scrap or rework the wafer, improving the process robustness and monitoring accuracy.

2. PROCESS FLOW

The patterning approach requires printing a minimum metal pitch of 28nm using an ASML 3400b EUV scanner. As shown in Figure 2, an SMO dipole source was used in this study to pattern vertical line space structures. The process starts with BEOL stack deposition on silicon wafers, followed by coating the wafers using metal oxide resist. EUV light (13.5) exposure and negative tone development (NTD) process was used to pattern trenches. This was followed by transferring the patterns into a 15nm TiN layer and then into a 60nm oxide dielectric layer using a different plasma etch conditions. The metallization step involved filling the trenches with 1.5nm TiN and ruthenium (Ru) followed by chemical mechanical polishing (CMP) to form electrically active Ru lines. CDSEM reference data was collected at ADI and AEI, while scatterometry spectra were collected at ADI, AEI, and post CMP. Resistance and capacitance of the Ru interconnects were measured by E-test.

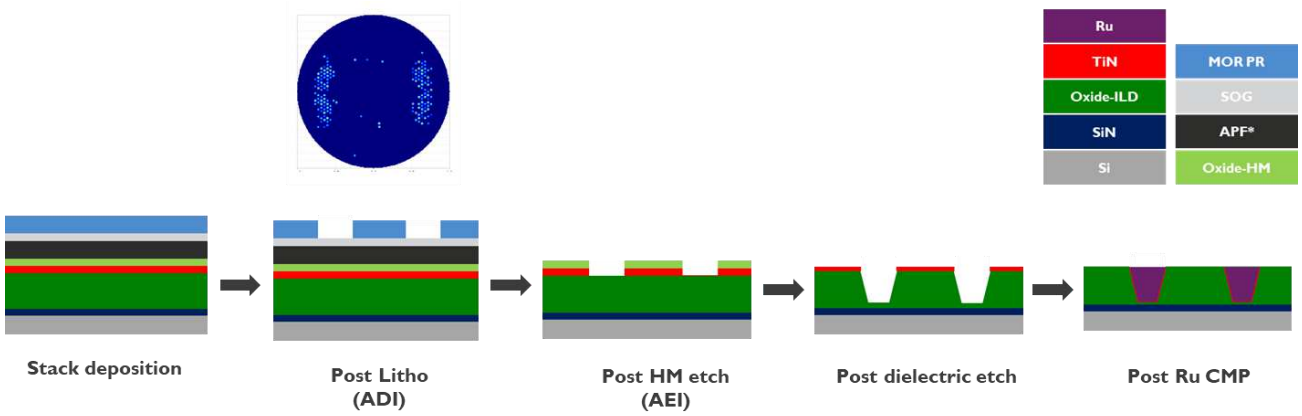

Figure 2 Process flow, stack and source map

3. RESULS AND DISCUSSION

3.1 Space CD measurements of 1D features

To produce a robust design of the experiment (DOE), we varied different process parameters at lithography and at etch steps. Lithography FEM (focus-energy matrix) and dose meander wafers were fabricated to obtain wide variation in the CD fingerprints. Table 1 shows the process conditions for different wafers.

Wafer id	Litho	Etch
D10	FEM	POR
D13	Dose meander	POR
D14	CDU	POR
D15	CDU	POR
D16	CDU	POR
D17	CDU	POR
D18	CDU	POR
D19	CDU	POR
D20	CDU	DOE
D21	CDU	DOE

Table1. Wafer process conditions at various steps

To ensure successful machine learning training (good training score), possible outliers need to be filtered from the reference data set. Reference data filtering was an essential aspect on the ML solution. The process window is small at these tighter dimensions, and lots of defects were observed on the CDSEM images when measured pictures were obtained outside the process window regime. Stochastic defects such as line bridges and breaks resulted in erroneous CD values while using the online CDSEM image-analysis algorithms.

Scatterometry spectra for ADI trench CD ML training were collected in the bulk line/space (LS) region. ML model was created using wafers FEM D10, Dose meander D13, CDU D14 and D15 (Table1) as training set wafers and tested on other CDU wafers. Figure 4 presents variability charts for all wafers. Mean CD values measured by ML solution on CDU wafers are comparable to the reference data. ML results show consistently smaller within the wafer (WIW) range. Wafer maps for FEM and CDU wafers are presented in Figure 3 for both CD SEM reference values and ML solution. There is a reasonable general matching of WIW patterns, with ML results showing a smoother map with fewer variations between the neighboring dies for the CDU wafer and the absence of the four dies with large measured CD values that are unexpected on the right side of the FEM wafer (larger dose).

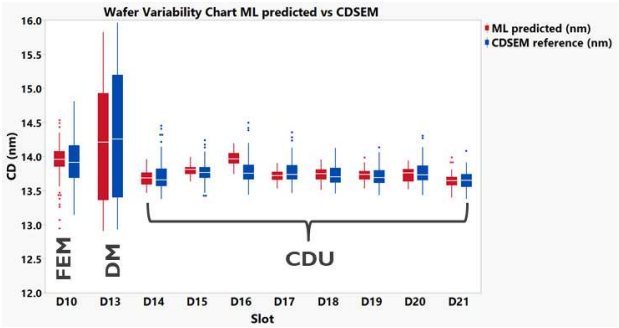

Figure 3. ADI variability chart for CDSEM reference and ML solution CD

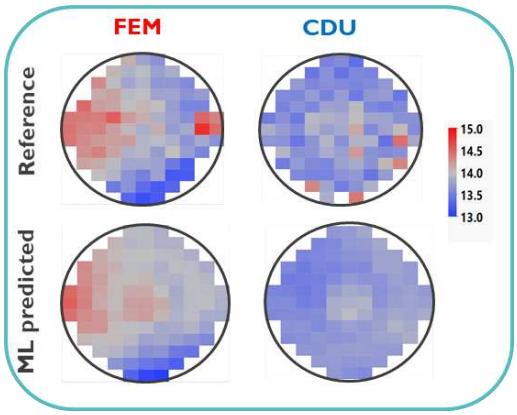

Figure 4. ADI wafer maps for FEM and CDU wafers: top CDSEM reference, bottom - ML solution.

Inline CDSEM data outliers were filtered also post HM etch to remove measurement errors caused due to line breaks and bridges. Scatterometry spectra for AEI ML training were collected from three different structures: fork-fork (FF) structures, meander (MR) structures, and bulk line/space (LS) region with 14nm CD and 28nm pitch. All structures and locations of the OCD and CDSEM reference measurements are presented in Figure 5. The fork-fork structure's width of the electrically active area is only 17 microns, which is much smaller than the scatterometry spot size (30 microns square). In the meander structure, the scatterometry spot size is comparable to the width of the device structure.

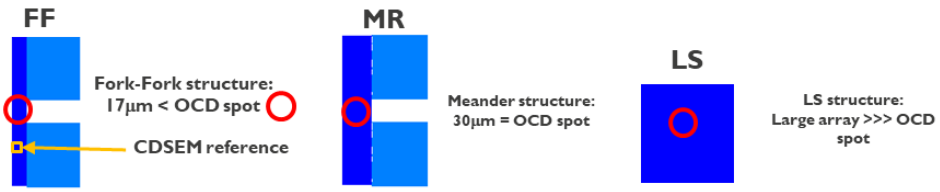

Figure 5. AEI measurement sites

A single ML model was created for all sites using wafers FEM D10, Dose meander D13, and CDU D14 and tested on all CDU wafers. Correlation plots are presented for each feature in Figure 6 (on top). We have separated all features to highlight the ML's capability to measure small targets:

comparing the R^2, the best correlation is for FF. This proves the ability of ML to measure targets much smaller than the OCD spot size accurately.

Wafer (D21) with much smaller trench CDs due to the modified etch process was also measured accurately by the ML solution, which shows ML solution capable of covering even unexpected process variation in the etch. The wafer maps are presented in Figure 6 (bottom) for two CDU wafers: both reference and ML solution show expected radial etch distribution of CDs for both etch conditions.

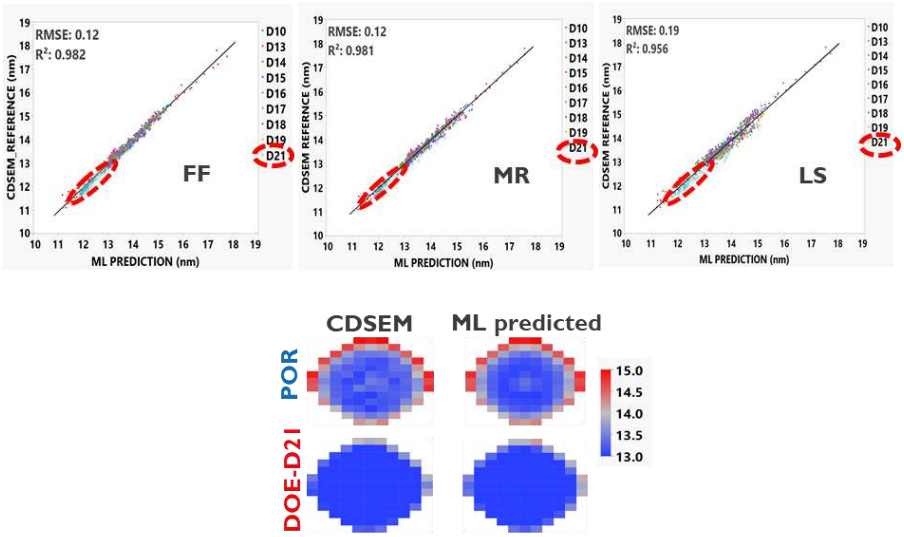

Figure 6. (Top) AEI Correlation plots between CDSEM reference versus ML prediction. (Bottom) AEI wafer maps for two CDU wafers (different etch conditions)

3.2 Tip-to-Tip (T2T) CD measurements of 2D features

The ability to directly print 2D features is a significant advantage of SE EUV compared to multi-patterning schemes and allows to simplify the process flow by eliminating block patterning, at least at some metal layers [8]. Usually, T2T measurements are done with CDSEM, which measures multiple single T2T structures to exclude measurement noise and capture variations of the T2T structures [8]. Unique test sites with different T2T structures were created to test OCD capabilities, including T2T variations and period and placement. The current study presents results for the test design consisted of 5 different T2T dimensions (22nm-26nm) between a staggered 60nm long islands. The test design schematic is presented in Figure 7A, and CDSEM images of the PR and HM patterns are shown in Figures 7B and C, respectively. The CDSEM measurement consisted of averaging 50 different T2Ts within one FOV for each location/die, and the average value was used to train the machine learning algorithm. The training was performed on FEM, dose meander, and CDU wafers for all five different feature sizes combined. ML solutions were trained for the ADI and AEI process steps.

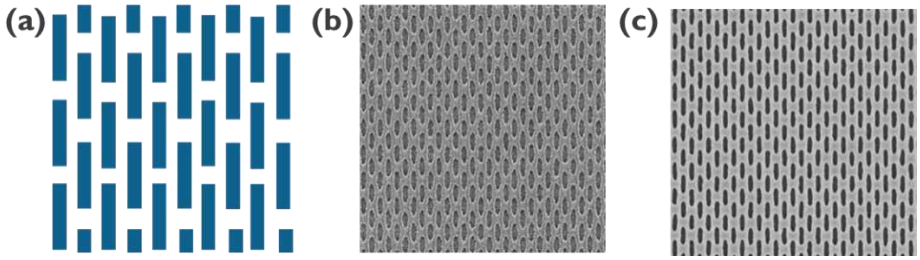

Figure 7. Schematic of the staggered block arrays (a) ADI printed pattern (b), AEI pattern etched into HM (c)

This solution was then used to verify each feature separately on the whole lot. When the predicted data were plotted vs. the reference data separately for each T2T case, we obtained a high R^2 value for both the ADI (Figure 8a) and AEI (Figure 8b) step, suggesting a good match to our reference data. It indicates that the OCD spectra signal could distinguish the slight variation considering the low T2T pattern density. Higher root mean square error (RMSE) values after etch are probably explained by wafer D21, which was etched with a non-POR recipe and was flagged in our correlation plots with different slopes (marked by green circles in Figure 8B).

Hence, OCD ML provides a fast and accurate inline monitor of the T2T metal line average value in ADI and AEI steps.

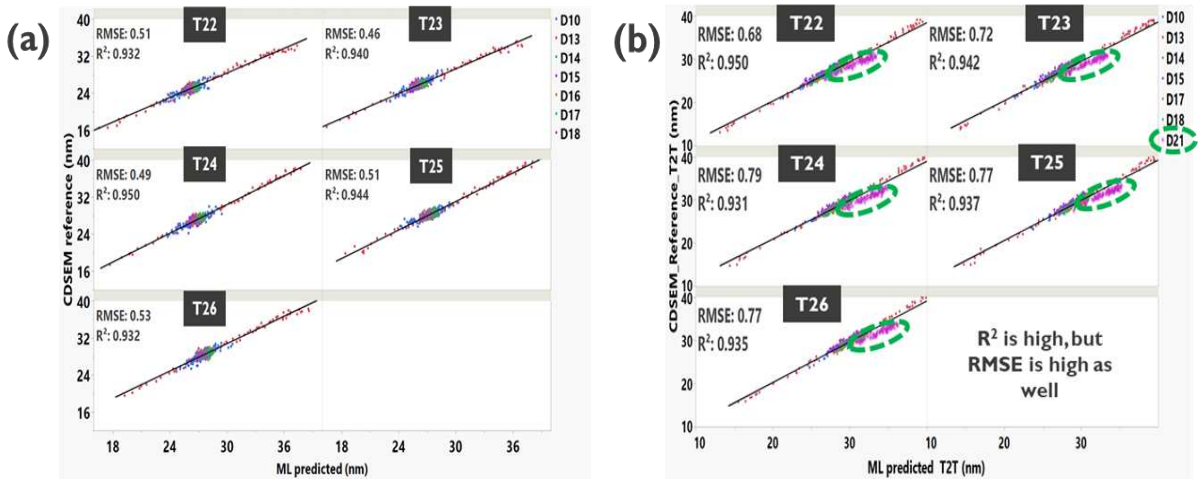

Figure 8. Correlation of ML predicted T2T values compared to reference CD values (a) ADI (b) AEI

LCDU of the T2T structures is also an essential parameter for the process control that CD SEM measures as a variation of the multiple T2T measurements at the same location. Analysis of measured LCDU values for our current structures and sampling based on 50 CDSEM T2T measurements showed large LCDU values (3 sigma around 10nm) that were almost not changing with our DOE conditions, as may be expected with dose variations. This behavior probably indicates the need for a more extensive sampling to enable accurate LCDU values as a requirement for ML training [9].

3.3 AEI LER measurements with ML

Reference CDSEM images were collected 49 times across the slit for different dose and focus conditions on P28 vertical line/space (LS) modules. The MetroLER software (v2.2.0) was then used to calculate the unbiased line edge roughness (LER) values. The machine learning training was done on two FEM wafers etched with two different etch recipes. LER data was collected in few columns (doses) with varying focus to maximize the LER range, as presented in Figure 9. Part of the data (two highlighted columns) was used for training the scatterometry spectra. Full map AEI unbiased LER estimation was also done on P28 vertical line/space (LS) modules using the ML solution.

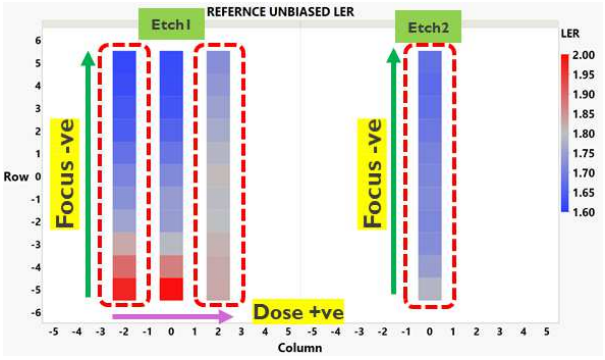

Figure 9. Reference unbiased LER values for two different FEM wafers calculated using MetroLER software (v2.2.0)

ML model was then validated on all measured dies and showed a correlation R^2 of 0.85 with a good RMSE of 0.03 for a small overall LER range (see Figure 10). It indicates that OCD ML prediction combined with the suitable reference input allows the well-predicted LER value at the AEI step.

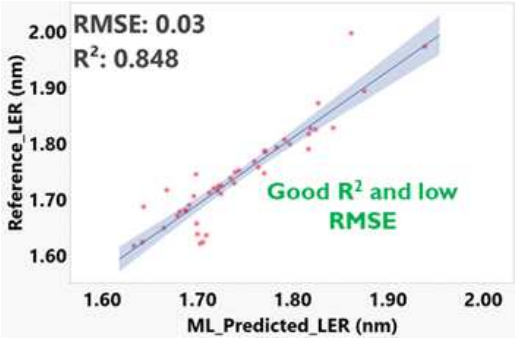

Figure 10. Correlation of predicted LER to reference LER values

After validation, we have used ML solution to predict wafer maps of both FEM wafers (see Figure 11). The LER range in the map is quite comparable to the split condition max range in the training set (1.6nm ~ 2.0nm for the max focus range). It is interesting that predicted maps show the expected small influence of dose on LER and expected better LER for the second etch condition. These prediction results prove that scatterometry with machine learning can measure unbiased LER with extensive sampling, much faster than the reference metrology.

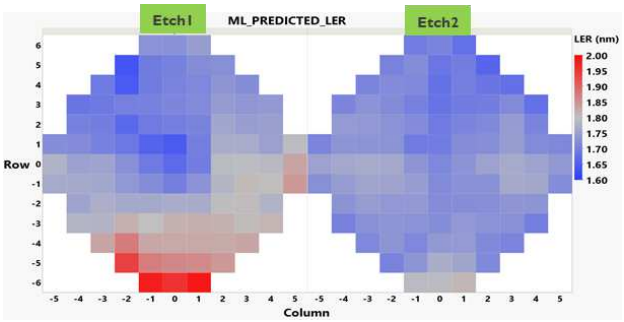

Figure 11. AEI LER wafer maps by scatterometry based ML solution

3.4 Etest prediction: Capacitance

After filling the trenches with ruthenium (Ru) and chemical mechanical polishing (CMP), the wafers were tested electrically. The FF structures were used for capacitance measurements. ML training was done separately for Pitch 28nm (14P28) and Pitch 30nm (15P30) structures. In the case of FF structures, the scatterometry spot size is bigger than the active device area's width, as mentioned before, and is demonstrated in Figure 12. When comparing the reference capacitance data to the ML predicted data, a good correlation score for both 14P28 and 15P30 fork-fork structures were obtained (see Figure 13a).

Correlation R^2 for the P30 structures is better compared to the 14P28 structures. One of the possible explanations may result from the more significant variability of P28 capacitance measurements due to defectivity.

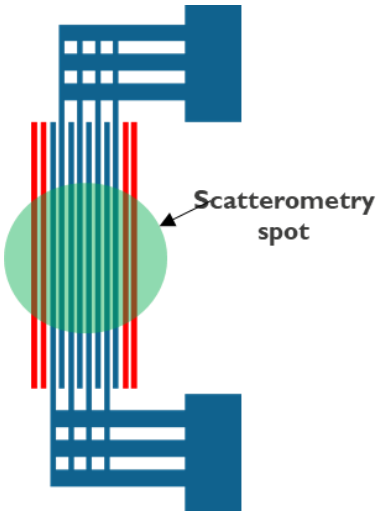

Figure12. Schematic of the FF size and the scatterometry spot size.

E-test measured wafer maps presented in Figure 13b shows an example of the unusual large capacitance value for the 14P28 structure compared to the neighboring dies (marked with the red circle in the center). This indicates a defective die, and a detailed defect inspection study is required to analyze the exceptional capacitance value. The ML predicted wafer map does not show this behavior. Hence, the relatively low R^2 of 14P28 and the mismatch points were mostly coming from the defective dies. It also shows that the scatterometry spectra are not sensitive to the small defects that can cause

erroneous capacitance measurements and could provide an overview in a wide range area with much less impact from defectivity.

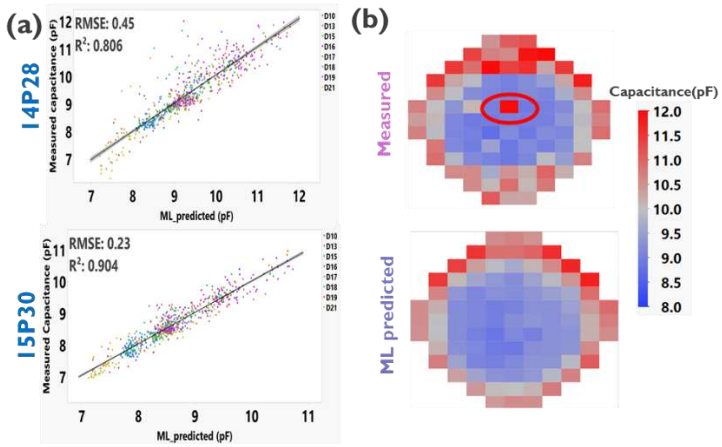

Figure13. Correlation plots between measured E-test and predicted capacitance values for 14P28 and 15P30 structures. (b) Capacitance wafers maps for 14P28 CDU wafer, measured (top) and predicted (bottom).

3.5 Etest prediction: Resistance

Resistance measurements were done on the meander structures, which have very long lines with multiple turns for resistance measurements (shown as a blue line in Figure 14), and dummy lines of the same CDs, that may be continuous (MR1) or cut into pieces (MR6). We present results for ML solutions that were trained for each one of the three structures (MR1 14P28 and 15P30, and MR6:14P28).

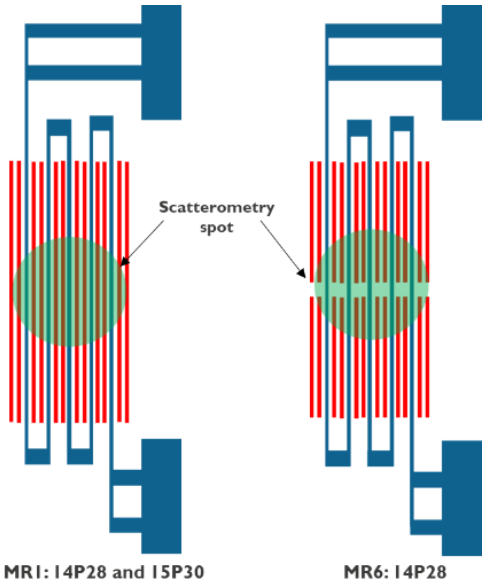

Figure14. Schematic of different meanders and the scatterometry spot size.

Predictions for all wafers showed good correlations to measured resistance values (R^2>0.93) in two pitches and two types of structure. The results are shown in Figure 15 below.

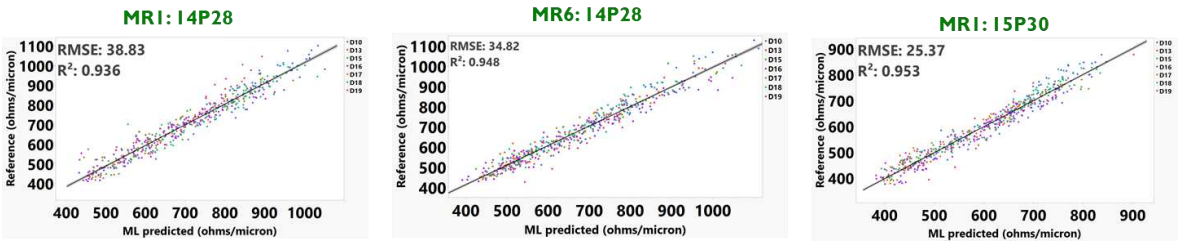

Figure15. Correlation between measured and predicted resistance values for three different devices

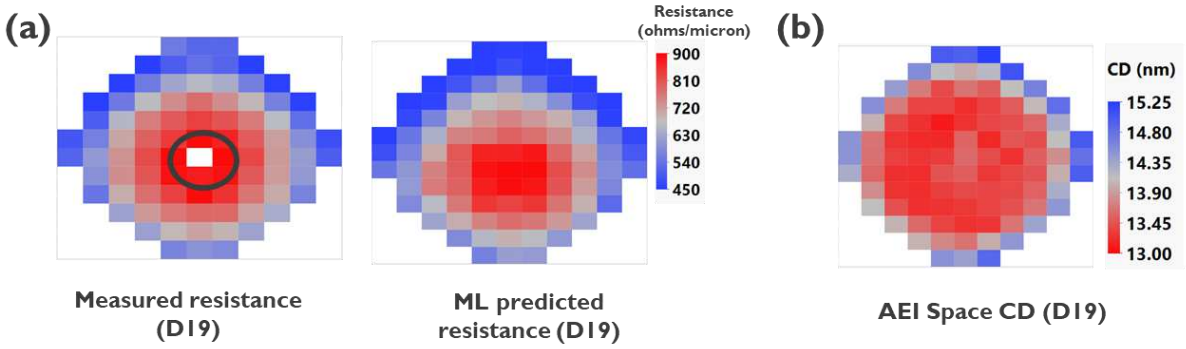

Figure16 Wafers maps: (a) measured and predicted resistance MR1 14P28 structure on a CDU wafer (b) space CD of the same wafer AEI

As expected, lower trench CD seen after HM etch in the wafer center showed higher resistance values. The highlighted die in Figure 16 showed an extremely high measured resistance value and was filtered out during the ML training. This can be due to a metal line break, and a detailed failure analysis study is required to understand the failure cause. ML solutions, on the other hand, predicted the Ru lines' electrical performance as if there are no defects, suggesting there is no sensitivity of the scatterometry spectra to defects.

CONCLUSION

Pitch 28 BEOL wafers were fabricated using EUV single print exposure with metal oxide resist and bright field mask. The damascene process was applied by using ruthenium (Ru) as metal lines. With ML solutions, scatterometry spectra demonstrated good capability for inline process monitoring after Litho (ADI) and HM etch (AEI) for various targets and parameters. Scatterometry measurements of line/space measurements, including CDs and unbiased LER, were verified and showed a good correlation in a small range. Tip to Tip variation in the staggered structure could be predicted by scatterometry ML solutions that speed up their measurement. It was demonstrated that targets smaller than the OCD spot size could be trained and verified accurately by ML solution. Beyond dimensional metrology, the scatterometry ML solutions post-CMP reveals excellent prediction of e-test measurements. Resistance and capacitance measurements were trained and validated on multiple meander and fork-fork structures, respectively. It was also shown that since scatterometry

measurements are not sensitive to small stochastic defects, the required ML training set needs to be carefully filtered due to their considerable impact on the referencing technique reading. Once correct training is performed, the ML solution can provide a prediction for locations where electrical measurements are compromised due to small defects.

REFERENCES

[1] N. G. Orji, M. Badaroglu, B. M. Barnes, C. Beitia, B. D. Bunday, U. Celano, R. J. Kline, M. Neisser, Y. Obeng, and A. E. Vladar "Metrology for the next generation of semiconductor device" Nat. Electron. Vol. **1**, page 662 (2018) doi:10.1038/s41928-018-0150-9.

[2] A. Vaid, B. B. Yan, Y. T. Jiang, M. Kelling, C. Hartig, J. Allgair, P. Ebersbach, M. Sendelbach, N. Rana, A. Katnani, E. Mclellan, C. Archie, C. Bozdog, H. Kim, M. Sendler, S. Ng, B. Sherman, B. Brill, I. Turovets, R. Urensky. "Holistic metrology approach: hybrid metrology utilizing scatterometry, critical dimension-atomic force microscope and critical dimension-scanning electron microscope" J. Micro/Nanolith. MEMS MOEMS Vol. 10(4), pp 043016-1-13, (December 2011). doi.org/10.1117/1.3655726

[3] P. Timoney, T. Kagalwala, E. Reis, H. Lazkani, J. Hurley, H. Liu, C. Kang, P. Isbester, N. Yellai, M. Shifrin, Y. Etzioni "Implementation of machine learning for high-volume manufacturing metrology challenges" Proc. of SPIE Vol. 10585, pp 105850X-1-8 (March 2018). doi: 10.1117/12.2300167

[4] D. Kong, R. Chao, M. Breton, C. Liu, G. R. Muthinti, S. Seo, N. J. Loubet, P. Montanini, J. Gaudiello, V. Basker, A. Cepler, S. Ng-Emans, M. Sendelbach, I. Kaplan, G. Barak, D. Schmidt, J. Frougier "Inline characterization of non-selective SiGe module defects with scatterometry enabled by machine learning" Proc. of SPIE Vol. 10585, pp 1058510-1-10 (September 2018). doi: 10.1117/12.2297377

[5] N Rana, Y. Zhang, T. Kagalwala, T. Bailey "Leveraging advanced data analytics, metrology solutions for advanced models to enable critical dimension machine learning, and metrology integrated circuit nodes, J. Micro/Nanolith. MEMS MOEMS, Vol. 13(4), 041415-1-9 (December 2014). doi.org/10.1117/1.JMM.13.4.041415

[6] Mary Breton, Robin Chao, Gangadhara Raja Muthinti, Abraham A. de la Peña, Jacques Simon, Aron J. Cepler, Matthew Sendelbach, John Gaudiello, Susan Emans, Michael Shifrin, Yoav Etzioni, Ronen Urenski, Wei Ti Lee, "Electrical test prediction using hybrid metrology and machine learning," Proc. SPIE Vol. 10145, pp.1014504-8 (12 April 2017); doi: 10.1117/12.2261091.

[7] S. Levi, I. Swrtsband, V. Kaplan, I. Englard, K. Ronse, B. Kutrzeba-Kotowska, G. Dai, F. Scholze, K. Anne, H. Johanesen, L. Kwakman, I. Turovets, M. Rabinovitch, S. Krannich, N. Kasper, B. Connolly, R. Wende, M. Bender, "A holistic metrology sensitivity study for pattern roughness quantification on EUV patterned device structures with mask design induced roughness," Proc. SPIE 10585, (2 August 2018); doi: 10.1117/12.2297265

[8] V.M. Blanco Carballo, J. Bekaert, M. Mao, B. Kutrzeba Kotowska, S. Larivière, I. Ciofi, R. Baert, R.H. Kim, E. Gallagher, E. Hendrick, L.E. Tang, W. Gillijns, D. Trivkovic, P. Leray, S. Halder, M. Gallagher, F. Lazzarino, S. Paolillo, D. Wan, A. Mallik, Y. Sherazi, G. McIntyre, M. Dusa, P. Rusu, T. Hollink, T. Fliervoet, F. Wittebrood "Single exposure EUV patterning of BEOL metal layers on the Imec iN7 platform", Proc. of SPIE 10143, 2017; doi: 10.1117/12.2258005

[9] D. Kong, D. Schmidt, J. Church, C.-C. Liu, M. Breton, C. Murray, E. Miller, L. Meli, J. Sporre, N. Felix, I. Ahsan, A. J. Cepler, M. Cheng, R. Koret, I. Turovets, "Measuring local CD uniformity in EUV vias with scatterometry and machine learning," Proc. SPIE 11325, (4 May 2020); doi: 10.1117/12.2551498