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Scatterometry based methodologies for characterization of MRAM technology

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ABSTRACT

Magnetoresistive random-access memory (MRAM) technology and recent developments in fabrication processes have shown it to be compatible with Si-based complementary metal oxide semiconductor (CMOS) technologies. The perpendicular spin transfer torque MRAM (STT-MRAM) configuration opened up opportunities for an ultra-dense MRAM evolution and was most widely adapted for its scalability. Insertion of STT-MRAM in the back end of line (BEOL) wiring levels has many advantages, including density, latency, and endurance with the promise of being comparable to performance of dynamic random access memory technology (DRAM). There are several important parameters at multiple process steps which require precise metrology for STT-MRAM integration. Inline metrology of the magnetic tunnel junction (MTJ) pillar is vital to calibrate the magnetic read/write performance parameters. This work discusses various challenges to monitor critical process steps for integrating STT-MRAM in advanced CMOS technologies and key metrology solutions are presented. To precisely predict MRAM junction resistance early in the process flow, a machine learning model was developed using scatterometry spectra collected after MTJ pillar formation and corresponding resistance data from the end of line electrical test. This machine learning model utilizes metrology data from the pillar formation process and can predict accurate device resistance values. Additionally, carefully monitoring the required planarization process of an interlayer dielectric deposited after the MTJ pillar formation is critical to avoid subsequent defects. Several modelling techniques are discussed and a new spectral interferometry-based technique, vertical travelling scatterometry (VTS), is demonstrated as a solution for measurements on fully integrated device areas.

Keywords: OCD, Spectral Reflectometry, Spectral Interferometry, VTS, STT-MRAM, Machine Learning

1. INTRODUCTION

Volatile working-class memories like static random-access memory (SRAM) & DRAM are critical components for data computation and processing with fast access time and long endurance cycles. Although volatile memory has very low latency and high switching speeds, increasing its density requires more power and/or space, which is usually a critical tradeoff in chip design to balance compute efficiency. Non-volatile memories, in contrast, have cost and density advantages with limitations on speed and endurance [1]. Non-volatile STT-MRAM technology promises fast programming speeds along with long endurance and is classified as an emerging memory with the potential to be a bridge between non-volatile storage class memory (HDD, Flash, etc.) and volatile working class memory (DRAM, SRAM, etc.). Research on memory technologies has been focused on improving the speed and endurance of spin-based MRAM to be comparable to that of the volatile working class memories like SRAM and DRAM [1,2]. STT-MRAM can be integrated with Si-based CMOS technologies with only three additional BEOL masks providing compatibility and cost advantages [3]. The state of an MRAM device is determined by reading the resistance values from a key component in the device called magnetic tunnel junction (MTJ) fabricated in the form of a pillar. MTJ pillars typically consist of a reference magnetic layer and a free magnetic layer separated by non-magnetic oxide. The direction of current flow through the MTJ influences electron spin polarization of the free layer, which determines the device's resistance state. When the magnetization direction of the free layer is parallel to the reference layer, the device is in a low resistance state and when the magnetization directions are in opposite directions, that produces a high resistance state. The difference between these states is called magnetoresistance and it should be relatively large to have a reliable measurement of the device's state [4]. Integration of these MTJ pillars

in the early BEOL metal levels is more complex than subsequent ones because of the need for scaled heights and reduced film thicknesses to fit in the available area. However, this integration scheme provides competitive cost, density, and electrical performance advantages [3].

The complexity of MTJ pillar integration at early metal levels drives the need for an effective metrology solution for process monitoring. The MRAM integration scheme begins with MTJ stack deposition followed by MTJ pillar formation. This MTJ pillar patterning starts with a hard mask (HM) etch followed by an ion beam etch (IBE) with in-situ encapsulation to form the MTJ pillar covered by a spacer. Unfortunately, even though ion beam etch (IBE) defines the MTJ pillar critical dimensions (CDs) and is a key process step determining MRAM device's electrical performance, in-line measurements are only possible after encapsulation. Previously published studies on MTJ pillar characterization focused on post-encapsulation critical dimension scanning electron microscope (CDSEM) measurements. The results required additional post IBE measurements on dummy samples to determine accurate pillar CDs independent of the encapsulant and correlate them to device conductance [5,6]. HM CD measurements before MTJ pillar formation do not capture any effects from etch processes. In this paper, scatterometry, also known as optical critical dimension (OCD), is used to demonstrate measurements of the MTJ CD post encapsulation on dedicated metrology targets. Scatterometry is a model-based technique that allows for measurements of the pillar CDs independent of the encapsulant and any process variations. In conjunction with machine learning models trained with electrical resistance data, scatterometry enables the prediction of device resistance at the earliest process step of the MRAM integration.

The MTJ integration scheme is then followed by inter-layer dielectric (ILD) deposition and subsequent chemical mechanical polish (CMP) to pattern the next metal level. Embedded MRAM integration requires uniform planarization across the wafer to prevent subsequent processing and integration issues [3]. ILD thickness measurements at multiple locations with different designs within a die are essential to monitor the planarization process variability. This work reviews the target structures with and without MTJ pillars and underlying logic across the die and the respective measurement techniques. It is challenging to accurately determine ILD thickness on active device arrays using traditional model-based OCD approaches because of the complex stack architecture including the underlying CMOS logic. Therefore, measurements on fully integrated devices are performed with the novel spectral interferometry-based vertical travelling scatterometry (VTS) technique [7]. It is found that non-destructive scatterometry is a highly suitable in-line technique that can measure ILD thickness within all desired areas with high throughput.

2. PROCESS DEVELOPMENT AND METROLOGY CHALLENGES

As device scaling continues along with integration of novel elements into the BEOL, metrology requirements are expanding to demand accurate monitoring of both metrology targets and active device areas for stricter control of the manufacturing processes. It is critical to monitor the MTJ CD for consistent and optimum MRAM device performance. Integration of STT-MRAM in BEOL CMOS logic starts with MTJ stack deposition and patterning as illustrated in Figure 1. The hard mask is patterned at nominal CD before etching the MTJ stack. An ion beam etch process is then used to form the final MTJ pillar profile followed by an in-situ encapsulation. The MTJ CD defines device resistance along with other factors including the MTJ layer stack, potential sidewall damage occurring during IBE and/or interface effects. Due to the in-situ encapsulation, in-line measurements are only possible either post hard mask open or post encapsulation. CDSEM can accurately measure HM CD and is used to monitor the patterning process; however, post encapsulation, it is difficult to differentiate the MTJ pillar from the encapsulant. Furthermore, in the case of pillar profile variations CDSEM analysis is very challenging especially when the MTJ CD is smaller than the HM CD [4]. Despite the disadvantages, typically HM CD or encapsulant CD with corrections are being used to monitor the process [5,6]. Nevertheless, it is critical to accurately characterize the MTJ pillar CD independent of profile and encapsulant to monitor the IBE process and predict overall device performance. If only the HM CD is used as an indicator, it may not capture the final CD or any variations such as notching, bowing, taper and redeposited material that might occur in the etch process [4]. Figure 2 shows a correlation plot of HM CD to electrical resistance measured across various device arrays grouped by their nominal embedded MTJ CDs (GP11 to GP32). Although there is a good correlation for the combined device groups with MTJ CDs spanning across a wide range of 60 nm, the correlation breaks down for short range individual CD groups. To address this issue, OCD solutions post encapsulation were developed to monitor pillar CD independent of encapsulant on dedicated metrology targets in the scribe line region. However, it is also important to measure on device arrays since it is known that the correlation to electrical test data is higher when scatterometry and electrical test data are collected on the same site [8].

Because there is an added complexity to develop a full geometric model for device arrays due to CMOS logic underneath, machine learning solutions were developed to enable high-efficiency optical metrology.

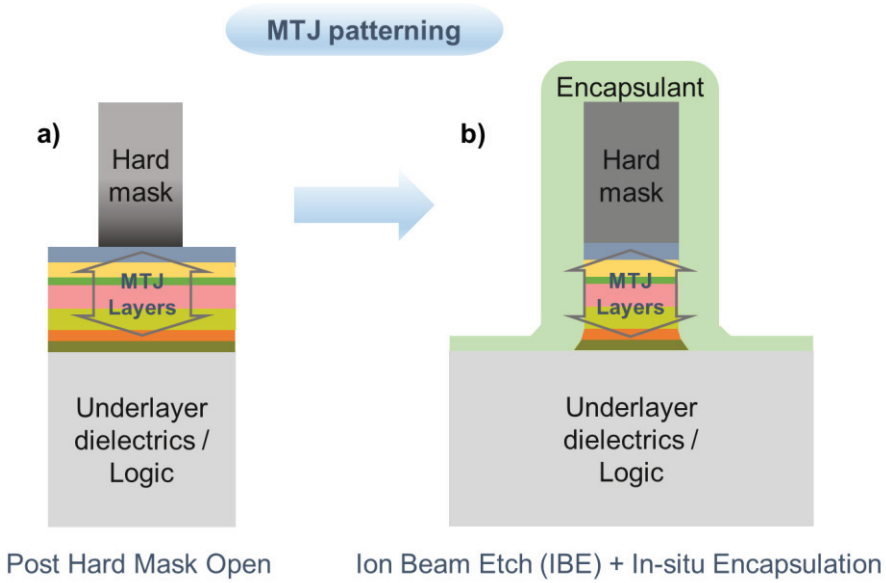

Figure 1. Schematic of active MTJ structures. (a) Structure post hard mask open; MTJ layers are not etched at this stage. (b) Same structure post IBE and in-situ encapsulation.

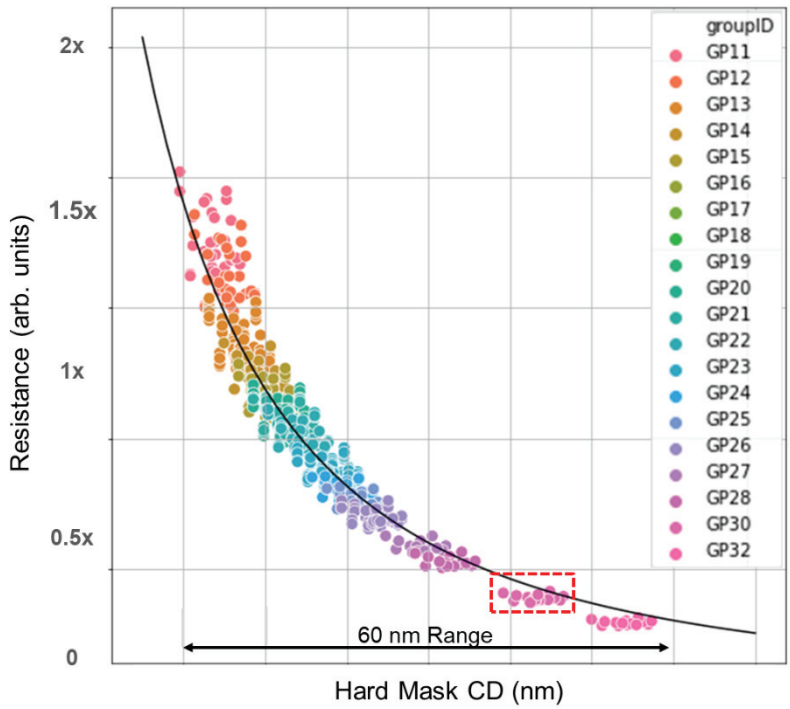

Figure 2. Normalized correlation plot of hard mask CD and electrical resistance for various MTJ CD groups (GP11 to GP32). The dashed box highlights one CD group (GP30) where almost no resistance change is observed even though the HM CD varies by about 10 nm. The range of plotted hard mask CDs spans 60 nm.

Another critical module post MTJ pillar formation is ILD CMP (Figure 3a). Uniform ILD thickness is essential to integrate MRAM between back-end metal levels. Non-uniformity in planarization or polish rate stems from pattern density, local pattern coverage, feature size or CD, pattern layout, and location of various macros designed in the die area [9]. This non-uniformity in ILD thickness can result in opens, shorts, and massive defects like copper puddles [3]. It is essential to measure these different die level segments to ensure uniform planarization across the wafer and monitor the CMP process in the most critical areas. Hence, an in-line metrology solution is required that can monitor all these multiple areas in a die. These different entities available for measurement can be categorized as metrology targets with and without MTJ pillars, device areas, and open areas (Figure 3b). The measurement targets vary in overall structure build and require different measurement and analysis schemes when using optical model-based techniques, for example. Metrology targets without underlying logic (with or without MTJ pillars) can be measured with OCD, and the spectra can be modeled using rigorous coupled-wave analysis (RCWA) methods [10,11]. A full build geometric model is no longer feasible for the targets with complex logic structures underneath. Therefore, a hybrid methodology is applied to measure open areas with logic underneath (no MTJ pillars). This hybrid methodology combines OCD spectra collected at pre-ILD deposition stage and post-CMP step to measure the ILD thickness [12]. Fully integrated device structures required implementation of a new spectroscopic interferometry-based technique, VTS, to selectively model only the top layers [7].

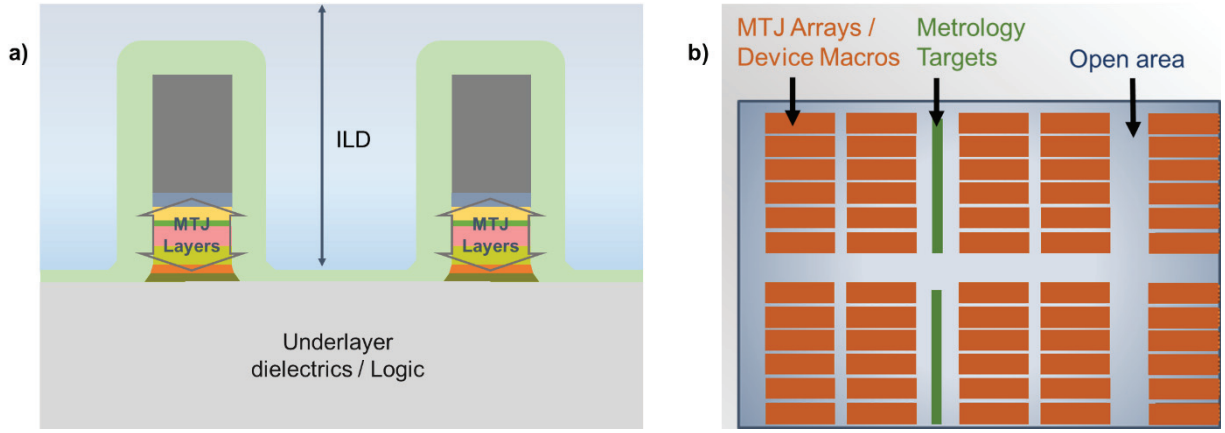

Figure 3. (a) Schematic of MTJ pillar with deposited ILD post planarization. (b) Schematic of a die area with device arrays (orange), metrology targets (green) and open areas (blue).

3. DESIGN OF EXPERIMENTS

3.1 MTJ Pillar Profile

HM patterning and MTJ stack etch are the two main processes that define MTJ pillars. As discussed earlier, the MTJ pillar CD is a key parameter that defines MRAM device resistance. In this work, five metrology targets (M2 – M6) were measured using a Nova T600 MMSR tool and analyzed using RCWA modeling methods. These targets have different nominal MTJ CD on similar underlayer dielectric layers. The nominal pillar CD varies within 20 nm and the optical model developed for these metrology targets is calibrated using transmission electron microscopy (TEM) images. The device arrays measured in this work (D1 – D7) have CMOS logic underneath and MTJ pillars of different nominal MTJ CDs embedded between M1 and M2 metal levels. Note that all measured targets are from wafers with nominally identical processing. CDSEM measurements post hard mask open were collected on a few MTJ HM pillars located in device areas (D1 – D2) for comparison and the correlation to device resistance was calculated. Nonetheless, measurements post encapsulation are essential to capture IBE effects on MTJ pillar. Since it is challenging to differentiate encapsulant from MTJ pillar using CDSEM, and a traditional OCD modeling approach is not feasible, machine learning (ML) solutions were developed using multichannel OCD spectra collected on a Nova T600 MMSR tool and end-of-line electrical results. This ML model can predict device resistance using incoming OCD spectra.

3.2 Interlayer Dielectric CMP Monitoring

ILD CMP monitoring requires ILD thickness measurements across multiple areas in a die consisting of various device and metrology targets. The measurement areas can be categorized into four different structure types as shown in Figure 4. A CMP split with four different levels is designed starting from least (CMP 1) to most aggressive polishing (CMP 4) to evaluate planarization dependency based on CMP condition and target type. A set of four wafers with identical processing till ILD deposition were run through CMP splits (CMP1 – CMP4) and measured across the above-mentioned available targets using a Nova PRISM tool. This tool has the added capability to measure absolute phase along with multichannel polarized reflectivity measurements [13]. Dedicated metrology targets (M1 – M3) with no underlying logic (Figure 4a,b) were analyzed using the traditional geometrical model build and RCWA approach. Figure 4c depicts active areas with logic underneath but no MTJ pillars. These structures (O1 – O2) can be modeled using a hybrid methodology. The impact from underlying logic is reduced by combining key information from spectra collected at pre-ILD deposition stage and spectra collected post ILD CMP process [12]. Hence a feed-forward methodology is set up where spectra from pre-ILD structure are included into a post CMP selective fit modeling scheme to solve the top ILD thickness. Fully integrated device structures (D1 – D7) as shown in Figure 4d were modeled using spectra from interferometry channels and VTS algorithms. The filtered spectral information and novel algorithms allow for selective modelling of the regions of interest while ignoring contributions from buried logic features [7].

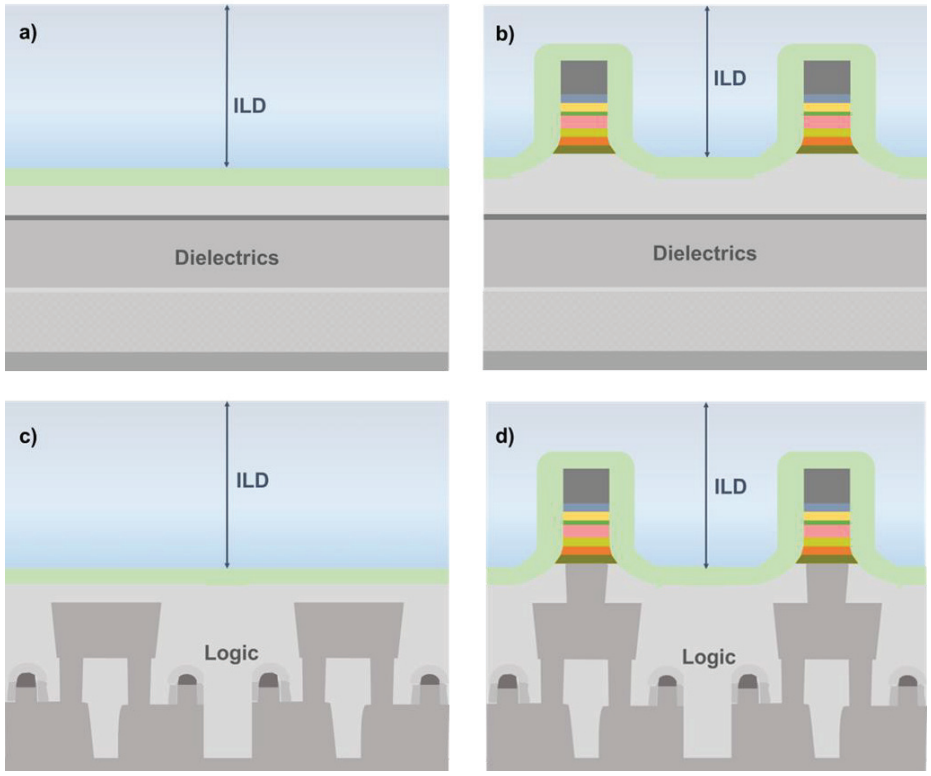

Figure 4. Schematics of different structural areas across the chip: (a) dedicated metrology target with no MTJ pillars and no logic devices underneath; (b) dedicated metrology target with MTJ pillars and no logic devices underneath; (c) active device areas with no MTJ pillars; (d) fully integrated device areas with MTJ pillars and logic devices underneath.

The set of samples associated with each experiment and the corresponding measurement techniques, modeling methods and target types discussed in this paper are listed in Table 1. A set of twelve wafers were identified to develop OCD solutions for IBE monitoring using metrology (M2 – M6) and active device arrays (D1 – D7) of different nominal MTJ pillar CDs. A set of four wafers were processed through different planarization conditions (CMP1 – CMP4) to measure ILD thickness across various metrology (M1 – M3), device with no MTJs (O1 – O2) and fully integrated devices (D1 – D7) and develop OCD solutions for uniform CMP development.

Table 1. List of samples and targets measured and analyzed in this work.

DOE	Target Type	Target #	Technique	HMO	Post Encap	Pre ILD Dep	Post CMP
MTJ CD Splits (12 wafers)	Metrology targets	M2 - M6	OCD RCWA		x		
	Fully integrated devices	D1 - D2	CD SEM	x			
	Fully integrated devices	D1 - D7	OCD ML		x		
ILD CMP Splits (4 wafers)	Metrology Targets	M1 - M3	OCD RCWA				x
	Device without MTJs / Open areas	O1 - O2	OCD Hybrid			x	x
	Fully integrated devices	D1 - D7	OCD VTS				x

4. RESULTS AND DISCUSSION

4.1 MTJ Pillar Profile Metrology

Normalized CD results from five metrology targets (M2 – M6), which differ only by nominal MTJ CD within a range of 20 nm are shown in Figure 5. A full geometric model was built to analyze the pillar profile using a standard RCWA methodology. The MTJ CD results without encapsulation show an excellent correlation to TEM reference data (Figure 5b). Such measurements can provide information about any process changes during pillar formation on dedicated metrology targets with no patterning underneath the pillars. OCD is a highly suitable technique that can capture actual MTJ pillar CD and profile on large arrays independent of the encapsulation and without sampling limitations.

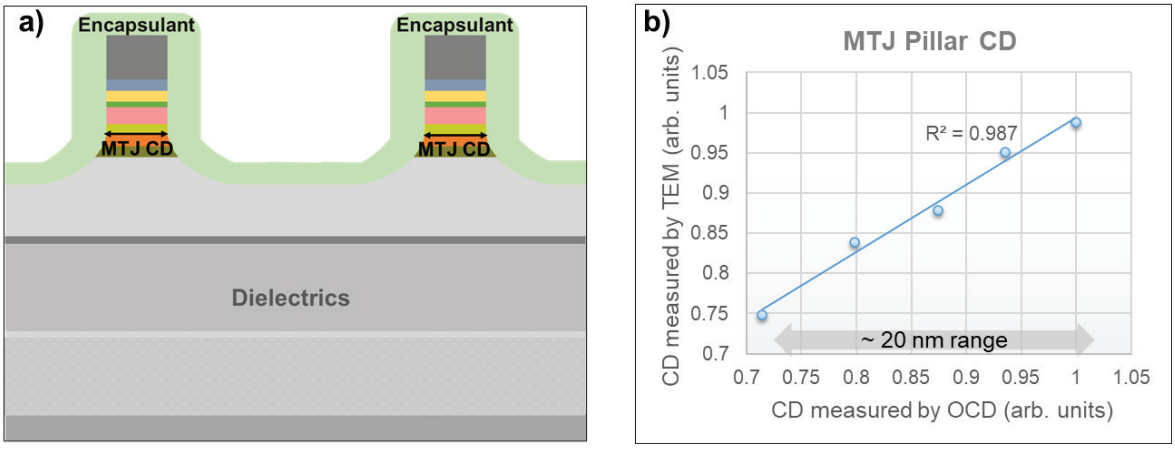

Figure 5. OCD results on metrology targets. (a) Schematic of a metrology target with MTJ pillars and no logic devices underneath. (b) Correlation plot of normalized OCD MTJ CD and TEM reference.

A different strategy has to be developed for fully integrated device target measurements, since a traditional optical model is infeasible due to the underlying stack complexity. For simplicity, CDSEM may be used, and Figure 6a depicts the correlation of HM CD to normalized electrical resistance for two fully integrated devices (D1, D2). While the device with a smaller CD (D1) does have higher resistance, it is noticeable that the correlation for individual device targets is poor even though there is a wide variation in CD. As discussed earlier, this is likely related to the subsequent IBE process, which determines the final MTJ pillar dimensions and profile. It should be noted that only a few pillars are captured within the field of view of a single CDSEM image, which may result in increased measurement uncertainty.

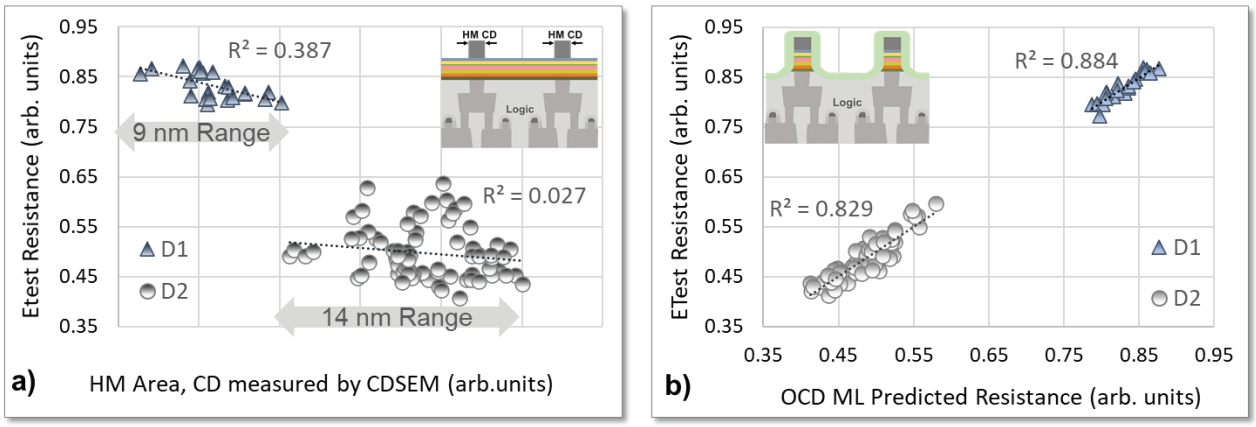

Figure 6. Normalized correlation plots of fully integrated device area measurements to electrical resistance. (a) Correlation plot of HM CD measured post hard mask open using CDSEM to electrical resistance. (b) Correlation plot of predicted resistance data from an OCD ML model post encapsulation and measured electrical resistance.

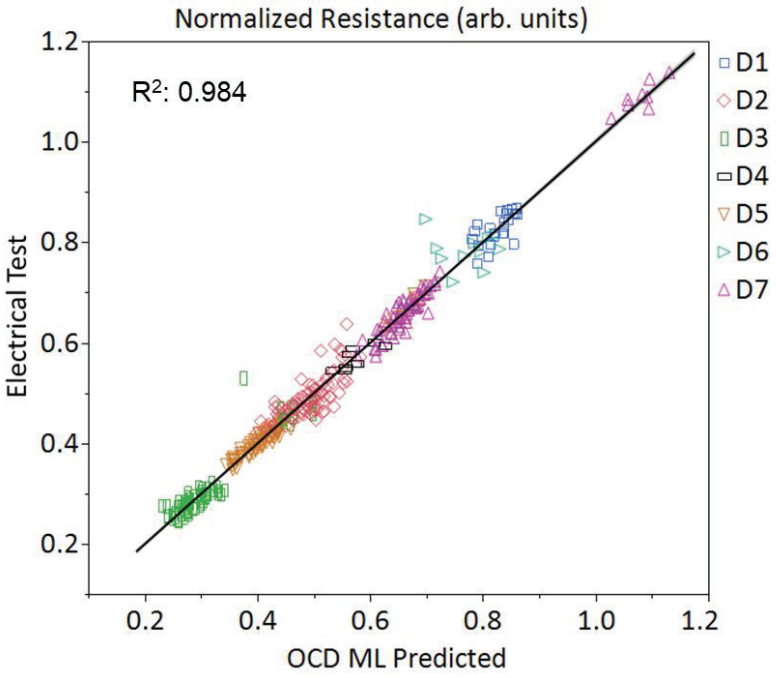

Figure 7. A correlation plot of normalized electrical resistance values and OCD predicted ML results for seven fully integrated device targets with different nominal pillar CDs.

Only a measurement after IBE processing will be able to capture any etch profile variations and potential secondary effects such as sidewall damage, for example. Optical scatterometry spectra carry all that information, however, creating a geometric model on fully integrated device targets is not feasible. Machine learning algorithms do not require a geometric model build and can help to obtain information not accessible with traditional approaches [14,15].

Therefore, OCD spectra are collected on device areas post encapsulation to detect any of the structural or material changes during the etch process. A machine learning model is developed to predict device resistance using reference data from in-line electrical measurements. Figure 6b shows individual correlation plots of OCD ML predicted resistance results to measured resistance data on two device targets (D1, D2). Note that the test and train datasets are not identical, which allows for an unbiased evaluation. The good correlation results confirm that the optical spectra carry IBE process information affecting device performance and that a ML model is capable of predicting device resistance well. The predicted OCD ML resistance has a significantly higher correlation to measured resistance than HM CD measured by CDSEM.

Training a ML model with a larger dataset reduces the proportion of variation and increases correlation to reference data. Seven different targets (D1 – D7) of various MTJ CDs within 30 nm across twelve wafers were trained with an excellent test on train validation ($R^2 = 0.99$; not shown for brevity) and cross-validation die level accuracy to electrical test results with $R^2 = 0.98$ (Figure 7). This machine learning approach can predict device resistance at the earliest accessible process step post pillar formation in a manufacturing line.

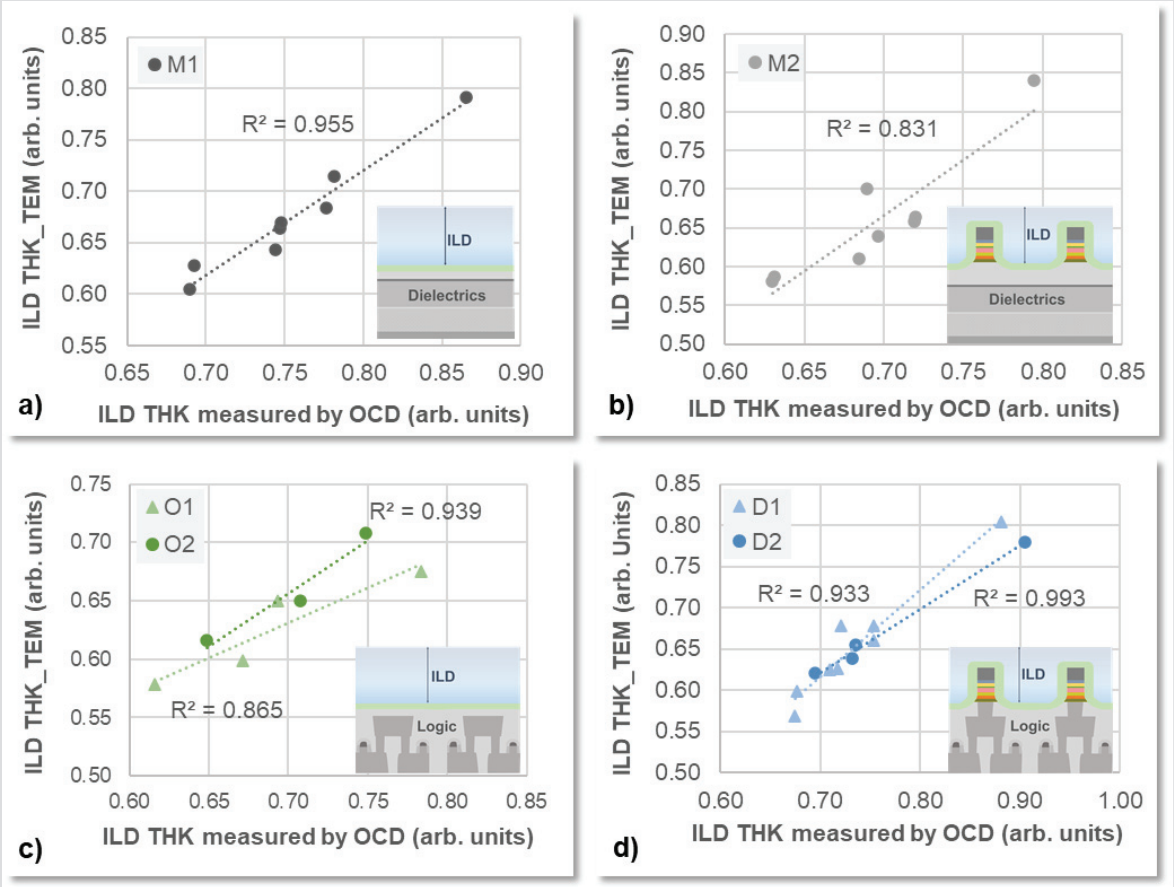

Figure 8. Normalized correlation plots of TEM reference data and ILD thickness analyzed by OCD using various modeling techniques. (a) OCD ILD thickness was analyzed using an RCWA method on metrology targets with no MTJ pillars. (b) OCD ILD thickness was analyzed using an RCWA method on metrology targets with MTJ pillars. (c) OCD ILD thickness was analyzed using a hybrid metrology method on active open areas. (d) OCD ILD thickness analyzed using VTS on fully integrated devices. The insets in each graph depict a schematic of the respective stack.

4.2 ILD Thickness Measurements Post CMP

Figure 8 shows normalized OCD results of total ILD thickness remaining on various structure types subjected to different CMP process times compared to TEM reference metrology. Normalized ILD thickness results on metrology targets (M1 – M3) with no FEOL logic underneath were analyzed using RCWA algorithms correlated to the TEM reference (Figure 8a,b). Normalized ILD thickness results on targets with FEOL logic underneath are presented in Figures 8c,d. Figure 8c shows ILD thickness results on areas with logic underneath and no MTJ pillars (O1 – O2) analyzed using a hybrid methodology. The selective fit solution is developed using spectra collected before ILD deposition and feeding key information to the final analysis with OCD spectra acquired post-CMP. Due to challenges mentioned earlier related to building a traditional optical model for device structures with integrated logic and MTJ pillars (D1 – D7), VTS was used to solve the remaining ILD thickness. The VTS technique enables measurements of the ILD thickness on fully integrated device targets without a full optical model (including the logic underlayers). Excellent correlation to reference metrology is achieved despite CMOS logic underneath (Figure 8d).

Figure 9 depicts ILD thickness results measured across the wafer on all the targets described in Table 1 (CMP Splits DOE). The results are separated by CMP conditions starting with least aggressive (CMP1) on the left to most aggressive (CMP4) on the right. As expected, with increasing planarization time the remaining ILD thickness decreases. For each CMP condition, a significant difference in ILD thickness can be observed between metrology targets (M1 – M3), areas without MTJs (O1,O2), and device targets (D1 – D7). While the difference between metrology targets without (M1) and with MTJ pillars (M2,M3) is due mainly to the presence of the pillars, it is important to note that these targets are not representative of the equivalent active O and D areas, respectively. For example, M1 cannot be used to monitor the ILD thickness in active open areas (O1,O2) as the location-dependent planarization variation has a significant impact. There is also a small but noticeable difference in ILD thickness between the seven fully integrated device macros based on pattern density and location across the chip. All OCD results show good sensitivity across these different macro types irrespective of CMP condition and can help to monitor location and density dependent thickness variations. This capability is useful for process development to optimize CMP planarization toward minimal non-uniformity across the wafer. It can provide high value in advanced manufacturing process control through on-device CMP monitoring.

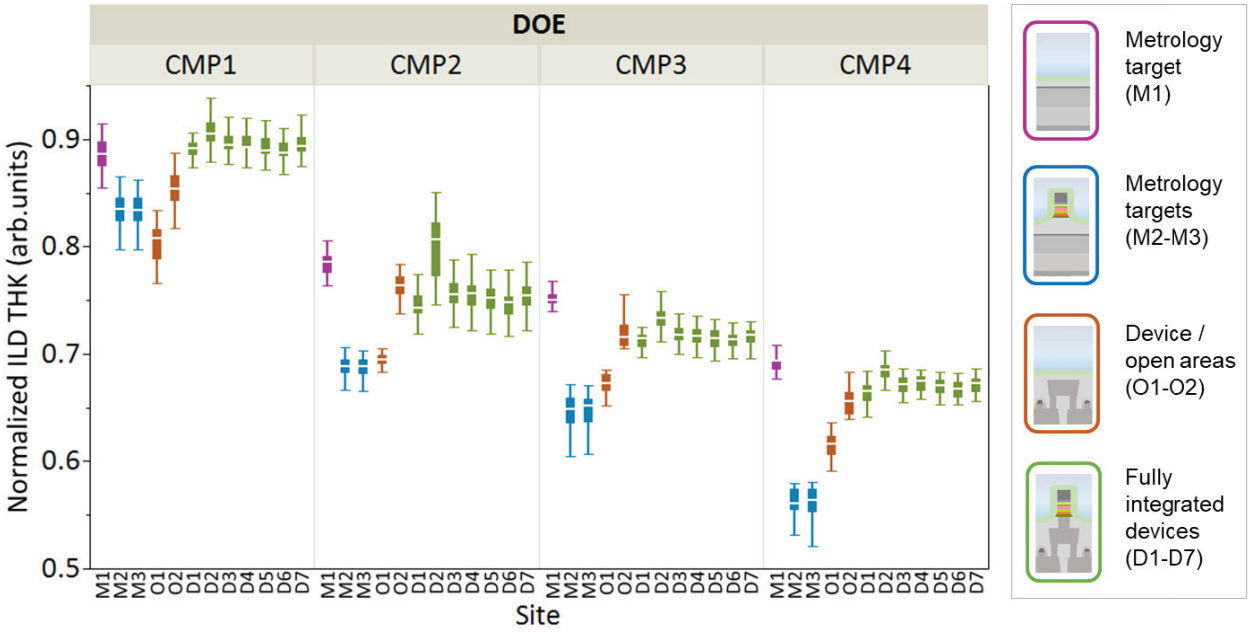

Figure 9. Cross-wafer normalized OCD ILD thickness results on various device areas, metrology targets, and active open areas from four different CMP split conditions.

5. CONCLUSIONS

This paper presents optical metrology solutions to monitor two critical STT-MRAM process steps: MTJ pillar formation and ILD planarization. MTJ pillar CD monitoring on metrology targets and in fully integrated device areas with logic underneath are presented and summarized. A scatterometry model which can solve for final MTJ CD and report CD independent of encapsulation is demonstrated on dedicated metrology targets. A machine learning solution is developed using optical spectra and in-line electrical measurements. With the advantage of quick time-to-solution, this ML approach provides significantly higher sensitivity than a traditional optical model and hence is an essential method to monitor IBE process variations in device areas. The ML predicted device resistance results showed an excellent correlation to resistance values measured at the end of the line. It is highlighted that for individual groups of device targets with a short CD range, ML offers a significant increase in correlation to electrical resistance compared to CDSEM HM measurements.

It is discussed that ILD thickness measurements on fully integrated device areas are critical for process monitoring and preventing subsequent defects. Monitoring the planarization process in various areas across the die is important for process uniformity determination. The possibility of ILD thickness measurements post CMP in device areas, open areas with logic underneath, and metrology targets with and without MTJ pillars is demonstrated using various scatterometry approaches. A new technique called VTS that combines spectral interferometry technology and novel algorithms to measure and analyze ILD thickness on fully integrated device structures with CMOS underneath was demonstrated. VTS results from device targets showed excellent correlation to reference metrology and enabled ILD thickness monitoring, which would not have been possible otherwise. The solutions discussed in this work overcome certain limitations from existing metrology solutions such as the influence of encapsulant, underlayer effects and sampling limitations. The methods discussed can be expanded and applied to other technologies [7].

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