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TSV Stress Evolution Mapping using in-line Raman Spectroscopy

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ABSTRACT

A comprehensive picture of the stress evolution within arrays of through-silicon-vias (TSV) is developed using in-line Raman spectroscopy. A set of wafers with different TSV geometries and metal seed liner thicknesses is exposed to various annealing conditions. Monitoring the Si-Si phonon mode shift between the vias, the influence of via geometries and processing conditions on the stress in the Si substrate is characterized non-destructively. Compressive stress is found in close proximity to the TSVs post Cu fill, as expected. However, for arrays with small TSV pitches, the substrate does not fully relax in the space between the vias, but rather tensile stress accumulates within the arrays. This inter-via stress increases with decreasing TSV pitch, accumulates towards the center of the arrays, and strongly depends on the annealing conditions. High resolution Raman maps within the arrays reveal the full picture of stress distribution in the TSV arrays. By using different excitation wavelengths, the variation of the stress with depth in the Si wafer is probed. The findings demonstrate the value of in-line access to process-dependent stress information. This knowledge helps to define design ground rules for highest device performance or to maximize the useable area on the wafer for logic devices.

Keywords: Through-Silicon-Vias, Stress, Raman Spectroscopy

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1. INTRODUCTION

Through-silicon-vias (TSV) present an essential enabling technology for heterogeneous integration [1]. However, the annealing procedure after Cu fill and overburden CMP creates mechanical stresses in the vicinity of the TSV which can negatively influence the performance of device structures close by or even lead to defects such as delamination of bonded wafers or wafer cracking [2,3]. Process-dependent TSV strain characterization is crucial to identify keep-out-zones where no critical devices can be placed, to optimize via placement, and define via-to-via spacings [4,5]. Theoretical studies use finite element methods to calculate stress around TSVs, but typically focus primarily on isolated TSVs due to high computation resource requirements, particularly when considering realistic geometries with multi-layer structures, patterning, or liners being present [6-10]. These calculations can predict general trends for stress modifications with major geometry changes but can hardly cover every process or subtle design change, and the complex stresses in larger arrays of TSVs. Nonetheless, experimental verification of any theoretical predictions is advisable.

Stress characterization in solid state devices can be done non-destructively using Raman spectroscopy [11]. Characteristic shifts of phonon modes proportional to the strain of the crystal lattice occur in the presence of stress. Using a small excitation laser spot, the stress distribution around features of interest can be determined with high spatial resolution. Here, we use in-line Raman spectroscopy to conduct a comprehensive study of the stress evolution in TSV test arrays by monitoring the Si-Si phonon mode shift between the vias. Utilizing different excitation wavelengths, strain at different depths in the Si wafer are probed, and results for different processing steps, via pitches, metal liner thicknesses, and processing conditions are presented.

2. SAMPLE DETAILS

Dedicated test wafers only containing TSVs with no other patterned features were produced for this study. Fig. 1 shows the process flow for the TSV formation in the oxide coated silicon substrate.

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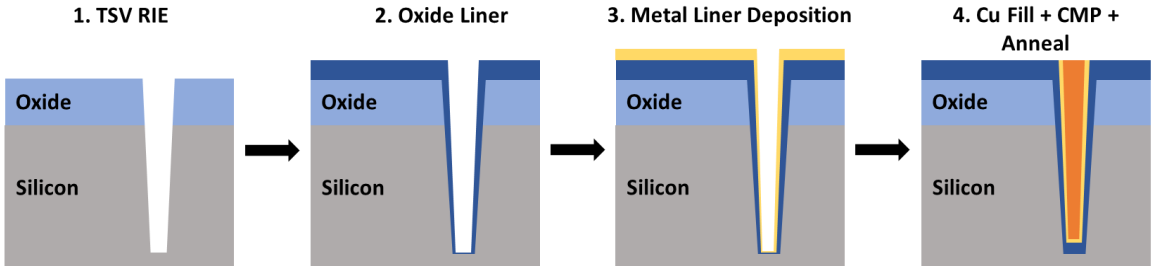

Fig. 1 Sequence of TSV processing consisting of TSV RIE, oxide liner deposition, metal liner deposition, Cu fill, overburden CMP, and an annealing step.

First, a TSV is formed by reactive ion etching (RIE), then oxide and metal seed liners are deposited, and the TSV is filled with Cu. Finally, chemical-mechanical polishing (CMP) is used to remove the metal overburden and the final structure is annealed. For this study, all TSVs have a nominal diameter of 10 µm and a nominal depth of 100 µm. The TSVs are arranged in square patterns of varying pitches. Here, test arrays of 26 µm, 40 µm, and 75 µm pitches are considered. A wide range of processing conditions were utilized in these experiments, including a variation of the metal seed liner thickness, varying annealing times including no anneal, and a range of annealing temperatures. The design-of-experiment (DOE) conditions included are summarized in Table 1.

Table 1 DOE conditions utilized in this study.

SAMPLE	DEPTH	DIAMETER	METAL LINER	ANNEAL TIME	ANNEAL TEMP.
A	100 µm	10 µm	Thin	None	None
B	100 µm	10 µm	Thin	Short	High
C	100 µm	10 µm	Thick	Short	High
D	100 µm	10 µm	Thin	Medium	High
E	100 µm	10 µm	Thin	Long	Low

3. RAMAN SPECTROSCOPY

Raman spectroscopy is commonly applied to non-destructively measure stress in Si-based semiconductor devices [11,12]. It relies on inelastic scattering of photons interacting with vibrational modes, the phonons, in the sample system. The presence of stress leads to strain of the Si-Si bond, which shifts the measured Raman mode characteristically. A review of stress characterization in electronic packaging using Raman spectroscopy is given by Ref. 13.

The stress distribution and direction around TSVs in Si is rather complex [14]. Compressive stress is expected along the axis of the TSVs and along the circumference of the vias. Tensile radial stress is predicted perpendicular to the TSV axis. A fully accurate treatment of the stress needs to consider all three components and respective descriptions are found in the literature [14]. Since the measurement geometry used here allows measurements only for one surface cut and with excitation along the surface normal, there is no sensitivity to separate out-of-plane from in-plane stress components and the often-applied approach of assigning a single value for the stress in the Si substrate is followed in this study. According to Tsang et al., the position of the Raman mode in Si in the presence of strain ε is given by [15]:

$$\omega_{\text{Si-Si}} = 520.2\ \text{cm}^{-1} - 815\varepsilon, \tag{1}$$

where the nominal unstrained mode position of 520.2 cm^{-1} is replaced in this study by the nominally unstrained value obtained from reference measurements in open areas away from any TSVs, which was generally found to be shifted less than 0.1 cm^{-1} from the nominal value. This approach was chosen to account for potential initial stress in the wafer. Assuming an elastic modulus, E, of 180 GPa for Si, the obtained strain value can be transformed to a value for the stress in the Si substrate using Hooke's law:

$$\sigma = E \cdot \varepsilon . \tag{2}$$

Raman measurements were performed in-line on a commercially available 300 mm wafer fab tool (Nova ELIPSON). This tool provides multi-wavelength capabilities to control the penetration depth of the excitation beam into the Si. Full and continuous polarization control allow maximization of the Raman scattering signal for any given material. For Si and considering the orientation of standard 300 mm Si wafers with notch along the <110> direction, the Raman tensor symmetry implies maximum scattering when both, polarizer and analyzer, are oriented within the {110} plane. A small spot size suitable for in-die characterization enables high-resolution measurements when set up as line scan or map.

Line scans of 1 µm step size were set up to cover several TSVs in each array, or entire arrays where possible. An example of the line scan over the 40 µm pitch arrays is shown in Fig. 2. Additionally, high-resolution maps were obtained for each pitch on one wafer with step sizes adjusted to measure approximately 1000 data points on a square around nine TSVs. The Si-Si bond related peaks in the raw experimental data were matched with parameterized line-shape functions which extract values for the center position of the peak, the amplitude, and the broadening.

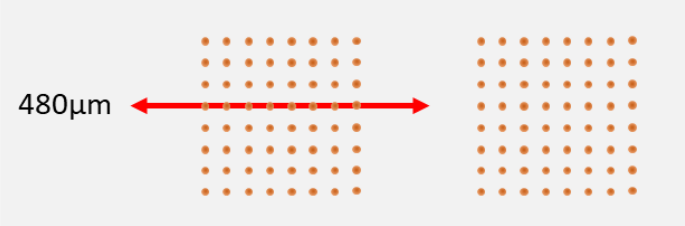

Fig. 2 Example of a line scan for the 40 µm pitch arrays. Dots indicate the position of the TSVs and the arrow symbolizes the scan direction for a 480 µm long line scan with measurement points spaced by 1 µm.

4. RESULTS AND DISCUSSION

Experimental peak parameters for a line scan between two TSVs in a 40 µm pitch array are shown in Fig. 3. The normalized amplitude of the Si-Si peak is constant between the TSVs and reduces only in close proximity to the TSV when the beam partially overlaps with the Cu vias. The peak width is not influenced by this partial overlap indicating accurate peak position determination close to the vias even in the case of partial beam overlap with the vias. For this scan, the Raman shift $\Delta\omega$ relative to the unstrained position is flat and close to 0 between the TSVs, and a strong increase of the Raman shift is observed near the TSVs. The observed amount of the Raman shift matches typical results in the literature for similar geometries. Going forward, the Raman shift will be translated into values for the stress in the Si substrate by combining Eqs. 1 and 2.

The stress evolution for three wafers measured after different processing steps is shown in Fig. 4. Line scans between the same two TSVs on a 40 µm pitch array were acquired after TSV RIE, after oxide liner deposition, and after Cu fill, overburden CMP, and anneal. Note, the metal coating over the entire wafer prevents Raman measurements after the metal liner deposition. The empty TSVs after TSV RIE and oxide liner deposition marginally strain the surrounding Si substrate resulting in essentially stress-free Si between the vias with slight tensile, i.e., positive, stress observed very close to the TSVs. Only the Cu filled TSVs after CMP and anneal show the expected compressive stress when approaching the TSVs. This stress is mainly a result of the different coefficients of thermal expansion between the Cu and the Si substrate [5]. Therefore, the amount of stress will depend distinctly on the processing conditions, especially

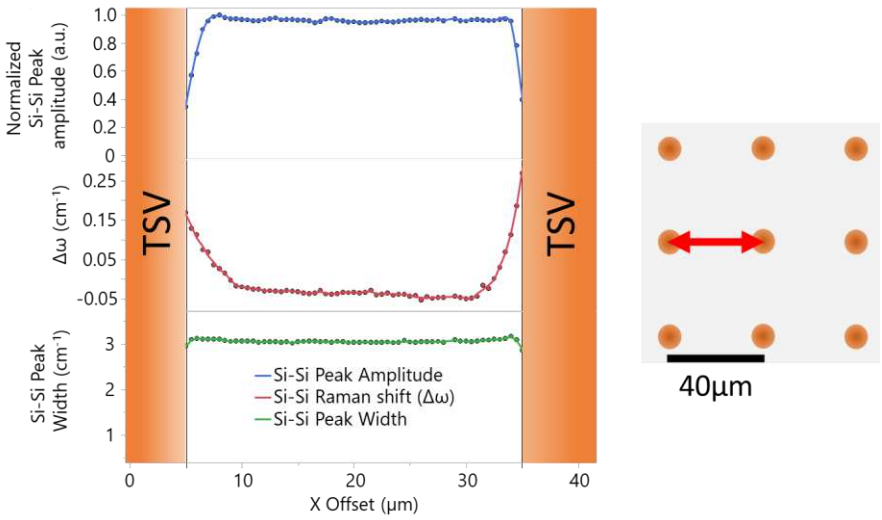

Fig. 3 Extracted peak parameters for the Si-Si bond for a line scan between two TSVs in a 40 μm pitch array as indicated in the sketch on the right. The normalized peak amplitude, Raman shift $\Delta\omega$ relative to the unstrained position, and the peak width are shown for the line scan between two vias of 40 μm pitch shown in the sketch on the right.

the annealing temperature and time. The observed compressive stress distribution close to the TSVs agrees with typical reports for the stress behavior near TSVs in Si substrates. However, note that the stress between the vias for this particular scan does not vanish. Instead, a mainly constant tensile stress remains between these two TSVs. This behavior contradicts the usual assumption that the stress relaxes entirely when measured sufficiently far away from any TSVs, typically more than 5μm.

To further investigate the tensile stress accumulation between TSVs, a line scan over an entire 40 μm pitch, square array of TSVs was set up, starting from an area of essentially stress-free Si, traversing over several TSVs, and ending outside of the array. A schematic of the line scan together with the respective stress distribution between the TSVs is shown in Fig. 5. Three regions of distinct behavior are identified: outside of the array and approaching the first TSV (1), between the first TSV and the center of the array (2), and from the center of the array to the opposite side outside the array (3).

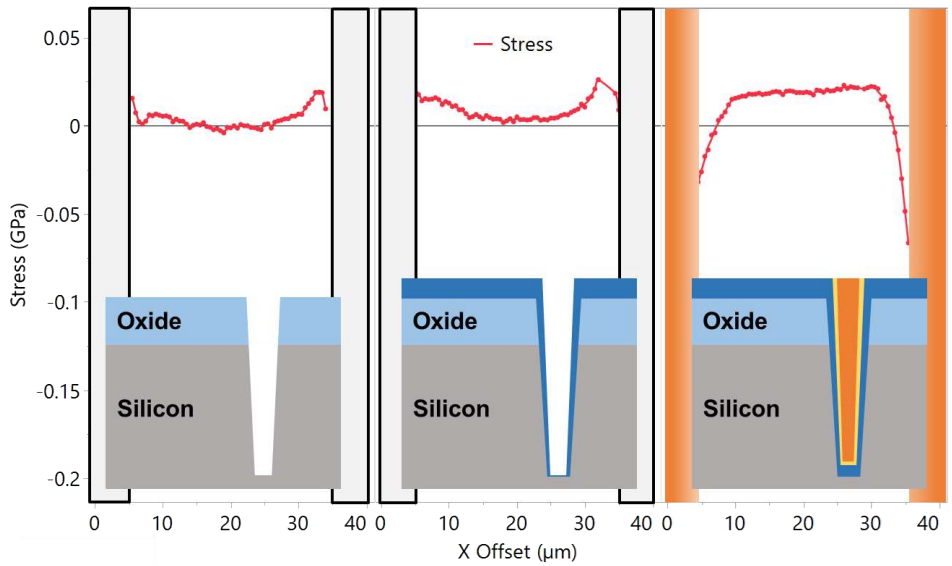

Fig. 4 Stress evolution for line scans between the same two TSVs in a 40 μm pitch array for wafers measured after different processing steps as indicated by the sketches in each column. The position of the TSVs is indicated by the columns at x = 0 μm and x = 40 μm, respectively.

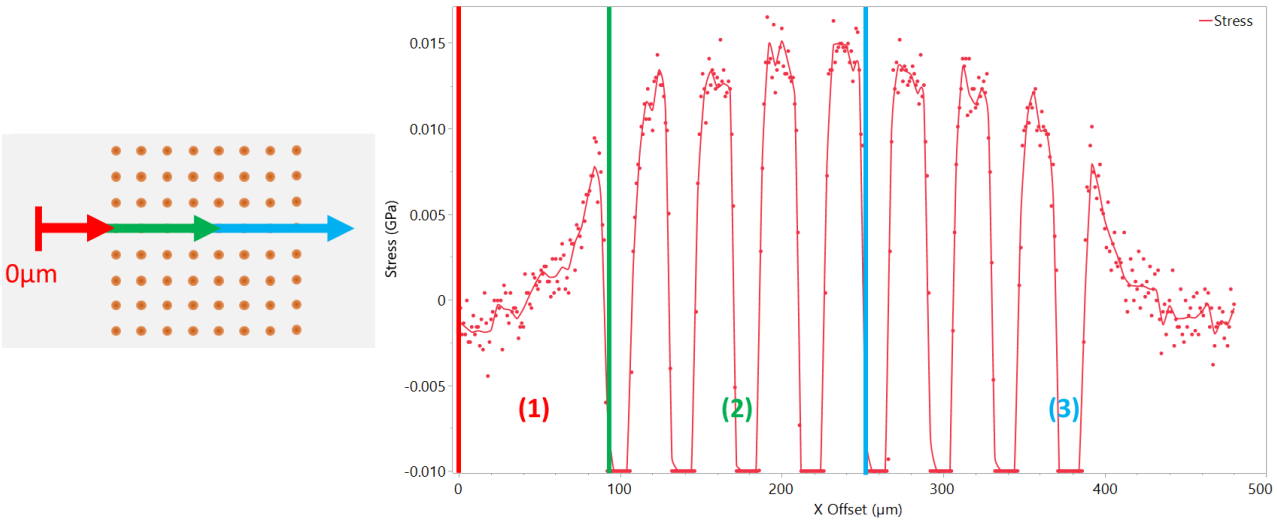

Fig. 5 Stress distribution for a line scan over a 40 µm pitch, square array of TSVs. Three regions are identified: outside of the array and approaching the first TSV (1), between the first TSV and the center of the array (2), and from the center of the array to the opposite side of outside the array (3). Note, the expected compressive stress very close to the TSVs is truncated at -0.01 GPa, resulting in a line of data points on the x-axis marking the position of each TSV.

In region 1, when approaching the first TSV from outside the array, instead of an immediate drop to negative, i.e., compressive stress values, a region of increasing tensile stress is observed first. Very close to the TSV, the typically expected compressive stress is observed. Since Cu blocks the Raman signal from the Si substrate in the TSV region, the data is truncated at -0.01 GPa in Fig. 5. On the opposite side of the first TSV (region 2), the compressive stress close to the TSV relaxes but does not level off in a stress-free state as typically reported for isolated TSVs. Instead, tensile stress is observed between the first and second TSV of the array. Further tracing the line scan to the center of the array, this tensile inter-via stress accumulated continuously. The maximum tensile stress observed at the center of this 40 µm pitch array is approx. 0.015 GPa which represents a 2× increase of tensile stress from outside the first TSV to the center of the TSV array. This behavior is mirrored in region 3, i.e. the tensile inter-via stress reduces steadily towards the edge of the array and only reaches a stress free-state far outside of the TSV array. While a tensile stress component is expected in the radial direction away from the TSVs, an accumulation in arrays of TSVs was not reported so far, to the best of our knowledge. Ryu *et al.* performed µ-Raman measurements on the edge of TSV arrays and found a tensile component between the TSVs [10]. They confirmed the observation with finite element calculations for the stress between lines of TSVs of similar pitch as studied here. However, measurement results for scans over an entire array of TSVs were not presented and essentially flat maximum tensile stress values between the vias with no variation past the first TSV pair were reported. Our results indicate that significant accumulation of tensile inter-via stress occurs when the TSVs are placed sufficiently close to each other. The lack of accumulation of stress within the array in the theoretical results presented by Ryu *et al.* might indicate that the effect of next neighbor TSVs is exacerbated in larger arrays.

A comparison of line scans over TSV arrays of different pitches is presented in Fig. 6. The stress distribution for square arrays of TSVs with 26 µm, 40 µm, and 75 µm pitch is shown. Accumulation of tensile inter-via stress is observed for each pitch. The amount of inter-via stress increases with decreasing pitch with maximum stress of approx. 0.025 GPa determined within the 26 µm pitch array. For the 26 µm and 40 µm pitch arrays, an approx. 2× increase of inter-via tensile stress is observed from outside the first TSV to the center of the array. Only in the array of largest pitch, a relaxation of the inter-via tensile stress is observed as a U-shape between the TSVs. For the finite element calculation results reported by Ryu *et al.*, a U-shape of the tensile inter-via stress was predicted even for smaller pitches [10]. The results for the smallest pitch studied here indicate maximum accumulation in the middle between the TSVs which contradicts the theoretical prediction. To confirm this behavior additional mapping scans were performed.

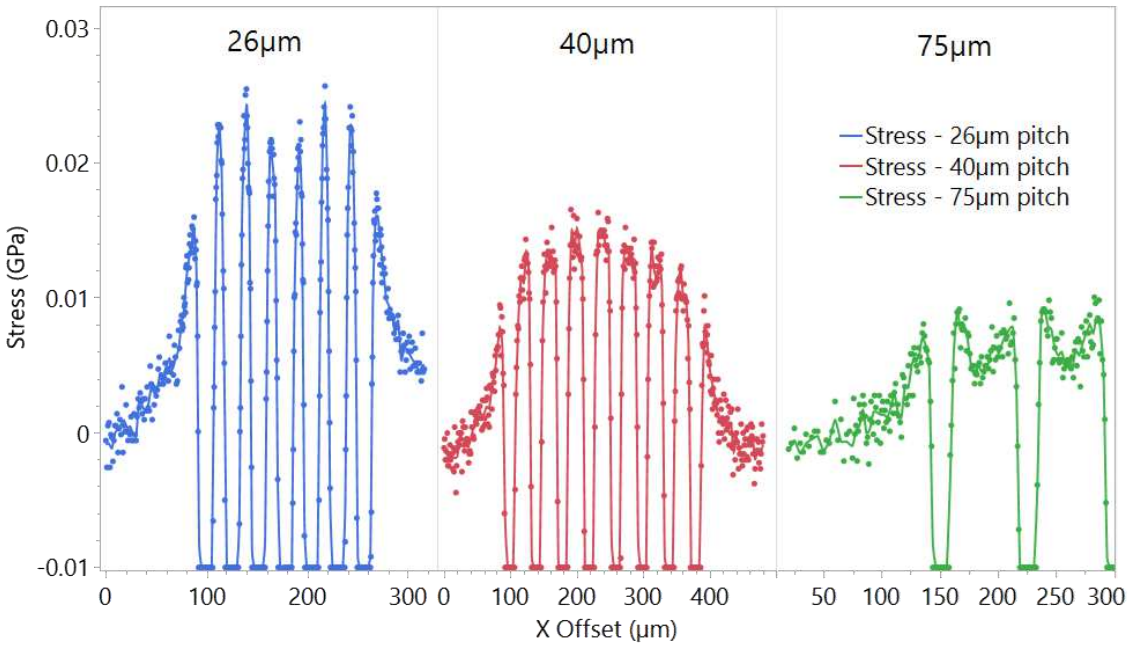

Fig. 6 Comparison of the stress distribution for line scans over square arrays of TSVs with 26 µm, 40 µm, and 75 µm pitch.

For visualization of the spatial stress distribution between the TSVs, 2-dimensional mapping data was acquired around 9 TSVs in the center of square arrays of TSVs with pitches of 75 µm, 40 µm, and 26 µm, respectively. The stress distribution for each of these high-resolution maps is presented in Fig. 7. The data was obtained from the same wafer and the same color scale is used for each map to allow comparison of the absolute stress values. The nominal position and dimension of the TSVs is indicated by black dots in each image. In close proximity to the TSV, the expected circular distribution of compressive stress is observed. For the 75 µm pitch array, little accumulation of inter-via tensile stress is found between the via, in agreement with the line scan results. The small tensile inter-via stress is limited primarily to planes containing the TSVs, resulting in a cross-pattern in the map. Stress vanishes in the interstitial areas between the TSVs indicating that device features placed in the interstitial areas would not be influenced by the presence of the TSVs nearby. For the 40 µm pitch array, the accumulation of tensile inter-via stress is much more pronounced. The four TSVs in the lower right corner of the map are located at the exact center of the measured TSV array. Darker shades of red between the TSVs in this area compared to the upper left corner of the map indicate that the tensile inter-via stress indeed accumulates towards the center of the array. As for the 75 µm pitch array, reduced stress is observed in the interstitial areas, but the stress in these areas does not vanish entirely for the 40 µm pitch array. In contrast to the 75 µm pitch maps, maximum accumulation of the tensile inter-via stress is determined in the middle between the TSV in agreement with the line scans. The highest tensile inter-via stress is determined for the 26 µm pitch array. Relatively high values of interstitial tensile stress compared to the 40 µm and 75 µm pitch arrays are observed everywhere between the TSVs, indicating that placement of critical device features between the vias has to be carefully considered. Literature references indicate that the absolute stress values could be reduced by decreasing the diameter of the vias which would be recommendable for the smallest pitch arrays of TSVs to maximize the useful array on the wafer without the need to consider the influence of the close-by TSVs on device performance.

Since the main source of stress around the TSVs is the difference in the coefficients of thermal expansion between the Cu and Si substrate, a strong dependence of not only the compressive stress close to the TSVs but also of the inter-via tensile stress on the processing conditions can be expected. Wafers annealed at different temperatures and for varying times were measured to investigate the stress evolution in dependence of varying annealing conditions. As indicated in Table 1, the available annealing conditions for this study ranged from no anneal, over short and intermediate length anneals at relatively high temperatures, to relatively short anneal at lower temperature. The stress distribution for different annealing conditions is shown in Fig. 8. Line scans were obtained on the same 26 µm pitch array of TSVs on different wafers exposed to varying annealing temperatures and lengths.

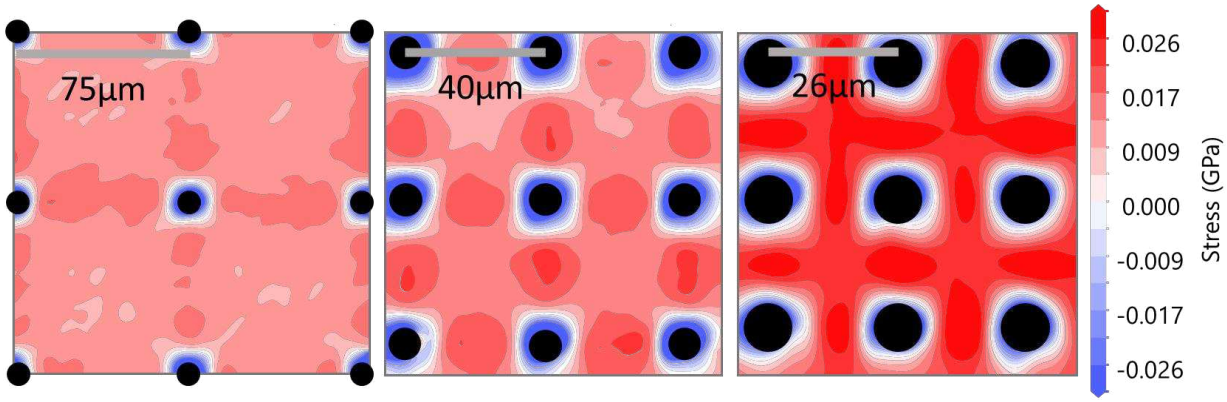

Fig. 7 Stress distribution for square maps around 9 TSVs in the center of square arrays of TSVs with 75 µm, 40 µm, and 26 µm pitch, respectively. Black dots indicate the position and nominal diameter of the TSVs. All three maps use the same color scale.

A clear dependence of the accumulation of inter-via stress on the annealing conditions is observed. The total amount of inter-via stress seems primarily governed by the annealing temperature. The lowest accumulation of tensile inter-via stress is found when the wafer was not exposed to further heat treatment other than during the initial Cu fill. A 2× to 3× increase of the maximum stress at the center of the array is seen for annealed wafers compared to no annealing. For identical temperatures, longer annealing times (indicated by a darker shade of red in Fig. 8) seem to result in higher stress accumulation though an eventual leveling of the maximum stress would be expected if the annealing length was further increased.

The effect of the seed metal liner thickness on the tensile inter-via stress is shown in Fig. 9. Line scans for two different liner thicknesses, thin and thick, for the same 26µm pitch square array is depicted. The line scans traverse the entire square array, some empty space, and end within a neighboring square array. In general, higher values of the tensile inter-via stress is observed for the thicker liner. While the stress in the space between the two arrays nearly vanishes for the thin metal liner, the thick metal liner wafer exhibits less stress relaxation between the arrays. Note, that the next neighboring array on the opposite side was sufficiently far away that no difference in the stress distribution is observed between the thin and thick metal liner samples at the beginning of the line scan. Qualitatively similar behavior was found for arrays of higher pitches, but the effect was most prominent in the smallest pitch arrays studied here.

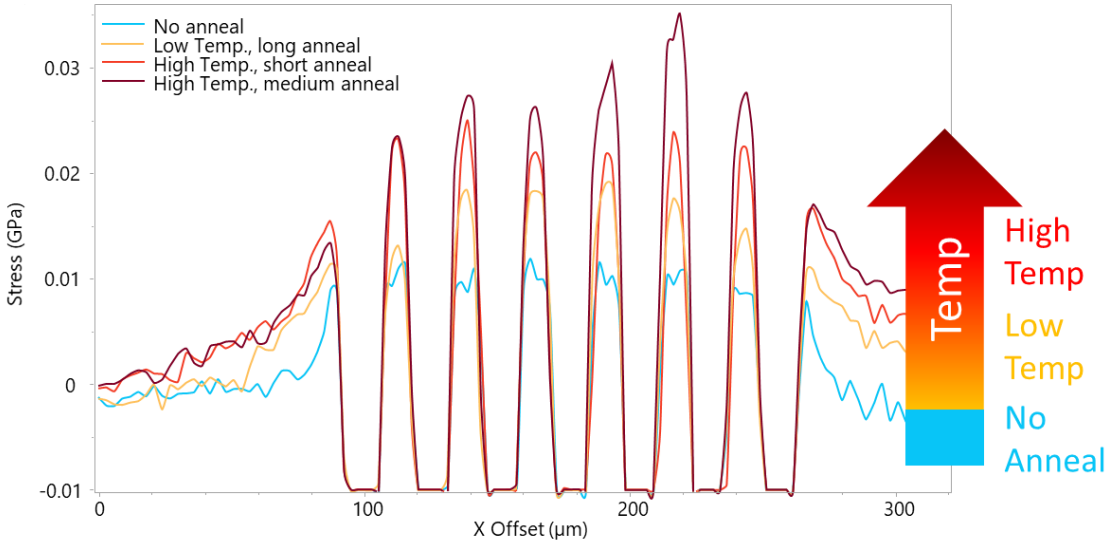

Fig. 8 Stress distribution for line scans over the same 26 µm pitch TSV array on different wafers exposed to a variety of annealing conditions ranging from no anneal to high-temperature annealing. Note, for the high temperature annealing step, two different durations were considered indicated by lighter and darker shaded of red.

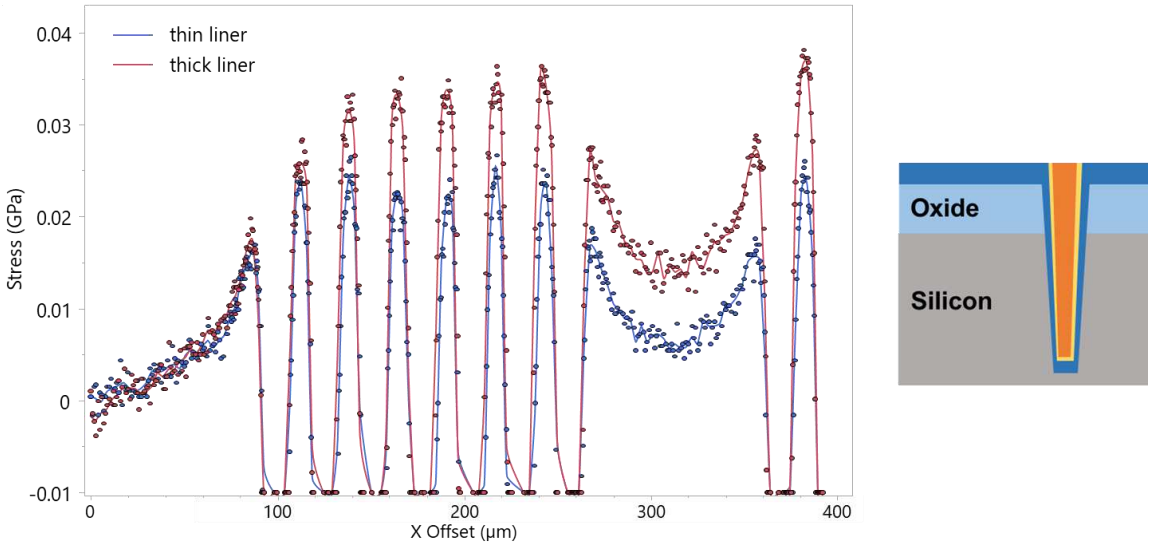

Fig. 9 Stress distribution for line scans over the same 26 µm pitch TSV array for two different seed metal liner thicknesses (indicated in yellow in the sketch on the right).

The penetration depth of the excitation laser depends on the selected wavelength. A long and a short excitation laser wavelength were selected to investigate the stress distribution around the TSVs depending upon depth. The penetration depth of the short laser wavelength in Si was calculated using Beer-Lambert's law to be approximately 100 nm, while the long laser wavelength was found to have a penetration depth of about 800 nm. A comparison of the stress distribution for line scans measured over the same 26 µm pitch TSV array using the two different excitation laser wavelengths is presented in Fig. 10. Higher tensile inter-via stress is found for the scan using the short excitation laser wavelength. This indicates that for the dimensions studied here, higher levels of stress are developed towards the surface of the sample. Presumably, the presence of the thick oxide layer on these samples and the resulting larger difference in the coefficient of thermal expansion between SiO_2 and Cu compared to Si and Cu contributes to the higher stress observed towards the surface of these wafers. The availability of several different excitation laser wavelengths on the Nova ELIPSON in-line Raman tool enables probing of stress at a depth most relevant for a given device structure.

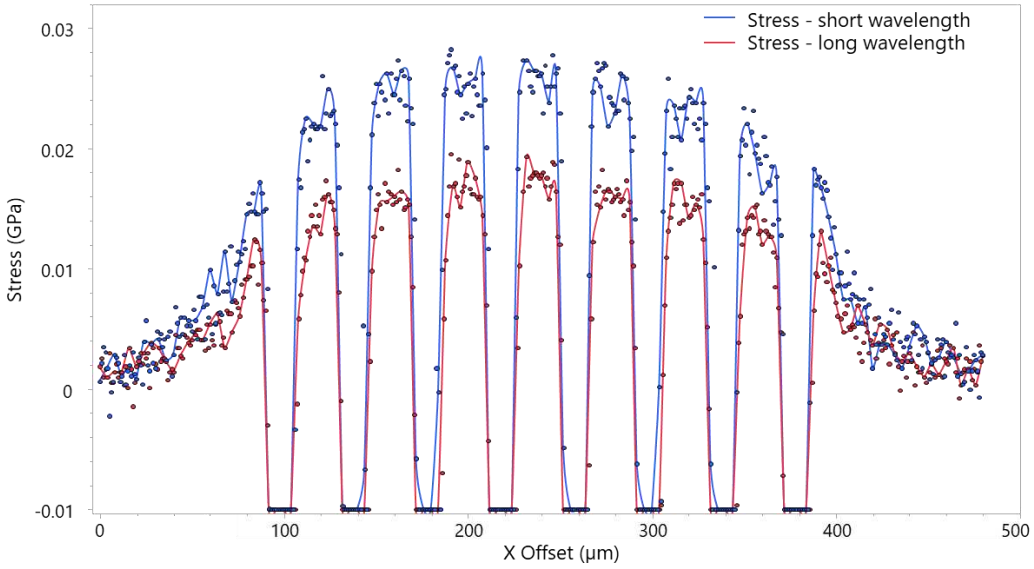

Fig. 10 Stress distribution for a 26 µm pitch TSV array obtained on the same wafer using two different excitation laser wavelengths. The longer wavelength laser light penetrates deeper into the Si substrates and thus probes stress at deeper levels than the short wavelength laser light.

5. SUMMARY AND CONCLUSIONS

In-line Raman measurements were performed to study the stress evolution in square arrays of TSVs. High-resolution line and mapping scans with a small excitation laser spot reveal the detailed distribution of the stress between the TSVs for different geometries and processing conditions. Strong compressive stress is observed in the vicinity of individual TSVs post Cu-fill and annealing in agreement with common expectations. In contrast to the common assumption that the stress relaxes completely away from the TSVs, an accumulation of tensile inter-via stress is found between TSVs arranged in square arrays. This inter-via stress increases with decreasing TSV pitch, accumulates towards the center of the array, and is strongest within the planes containing the vias with reduced stress in interstitial spaces. The amount of stress is found to increase with the thickness of the metal seed liner. Further, inter-via stress accumulation within the arrays strongly depends on the annealing conditions with higher temperatures and longer annealing times generally leading to larger tensile inter-via stress. The selection of different excitation laser wavelengths allows stress to be probed at relevant device feature depth due to different penetration depths. An increase of the tensile inter-via stress towards the surface was observed for the samples under investigation in this study.

In conclusion, the stress around TSVs arranged in square arrays varies considerably based on design and processing conditions. An accumulation of a tensile stress component is observed between the vias in these arrays in addition to the strong compressive stress expected in close proximity to the TSVs. While the absolute values of stress between the vias for individual design and process changes discussed here such as decreasing pitch, increasing liner thickness, or higher annealing temperatures, might not seem high enough to have a significant influence on the performance of critical devices nearby, the combined effects can add up significantly, and acceptable amounts of stress can vary for different device structures. Since accurate predictions of total stress for large TSV arrays and complicated layer structures found in modern devices are difficult if not impossible, access to accurate stress measurements using Raman spectroscopy becomes valuable for development but also in-line monitoring. While high-resolution line and map scans are not feasible for in-line monitoring, the results presented here give a good idea where within the TSVs stress monitoring might become necessary. General trends of shrinking TSV diameters and reduced liner thicknesses will help to mitigate the effects of increasing inter-via stress due to shrinking TSV pitches which will allow the usable area to be maximized for device structures on production wafers.

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