

In-line XPS metrology for area-selective deposition processes on patterned structures

Manasa Medikonda^{*a}, Linda Wangoh^a, Christopher J. Lee^a, Mark Klare^b, Dimitry Kislitsyn^b, Heath Pois^b, Paul Isbester^b, Aron Cepler^b, Wei Ti Lee^b and Daniel Schmidt^a

^aIBM Research, 257 Fuller Road, Albany, NY, USA 12203

^bNova Inc, 3342 Gateway Blvd, Fremont, CA, USA 94538

ABSTRACT

Area-selective atomic layer deposition (AS-ALD) processes are gaining significant traction as advanced technology nodes demand improved edge-placement accuracy and atomic scale process control. These selective deposition processes enable a bottom-up fabrication approach without lithographic or subtractive patterning methods, offering a viable approach to address significant challenges posed by scaling logic technology beyond the 3 nm node. A class of materials called self-assembled monolayers (SAM) are most widely studied for area-selective deposition (ASD) for their ability to deactivate ALD growth selectively. SAM chemistries can be tailored to selectively adsorb only on specific materials while remaining inactive on others, thereby allowing surface dependent ALD growth. Achieving robust selectivity and accurate characterization becomes especially challenging on patterned structures, where feature dimensions are extremely small and the growth and non-growth regions are positioned in immediate proximity. It is vital to measure these ultrathin growth layers and monitor the deposition processes inline to ensure that area-selective growth occurs only in the intended regions. Additionally, if SAM and back-end-of-line (BEOL) stack materials share identical elemental signatures, conventional inline metrology techniques are unable to distinguish their contributions separately. These limitations create a critical need for a non-invasive measurement method equipped with novel advanced analytical algorithms capable of resolving angstrom level thicknesses.

In this study, gas phase SAMs were selectively adsorbed onto patterned BEOL Cu wires, after which TaN was subsequently deposited through multiple ALD cycles. The Cu line structures were fabricated with intentional line and space design variations to evaluate pattern dependent behavior. The AS-ALD process conditions were also varied to assess their impact on the SAM layer and its effectiveness as a selective growth barrier. Inline X-ray photoelectron spectroscopy (XPS) measurements in combination with advanced algorithms and a feed forward analysis framework were utilized for evaluation and quantification of selective deposition processes on patterned structures. This approach enabled accurate extraction of SAM and TaN thicknesses on both growth and non-growth areas, thereby providing a reliable basis for calculation of selectivity metrics. Additionally, newly developed algorithms facilitated the resolution of SAM derived signal from BEOL dielectrics even when the elemental compositions are identical.

Keywords: In-line XPS, advanced XPS, AS-ALD, ASD, SAM, area-selective deposition metrology, bottomless barrier, BEOL metrology, metrology, Cu interconnects

*Corresponding author: manasa.medikondal@ibm.com

1. INTRODUCTION

Front-end-of-line (FEOL) transistor scaling requires proportional scaling of corresponding back-end interconnects to sustain system level performance [1]. However, continued back-end-of-line (BEOL) pitch reduction presents fundamental scaling challenges that increasingly limit interconnect performance and scalability. Empirical data indicate that continued reduction of BEOL interconnect dimensions lead to increased line resistance [2,3]. Key contributors to this trend include the reduction in interconnect line width and the presence of diffusion barrier and liner layers, which are required to prevent copper diffusion into the surrounding low-k dielectric materials [4]. At advanced technology nodes, these barrier and liner layers consume a disproportionately large fraction of the total metal cross-section compared to earlier nodes [5]. As the effective copper volume decreases, the resulting reduction in conductive area leads directly to higher line resistance [5]. In addition to resistive penalties, aggressive pitch scaling results in closely packed wiring, which increases parasitic

capacitance between adjacent lines. The combined increase in resistance and capacitance results in undesirable RC delay, further degrading signal propagation speed and overall device performance [6]. Manufacturing complexity also increases at tight pitches. Transitioning from a strictly top-down patterning approach to more bottom-up, self-directed processes has the potential to reduce process complexity [7]. To address these limitations, particularly those associated with barrier and liner scaling, new interconnect integration schemes and process solutions are required. Such approaches must enable continued extension of copper interconnect technology while also providing pathways to reduced resistance, simplified process flows, and potential adoption of next-generation interconnect materials [1,7].

One promising approach to address the increasing resistance associated with aggressively scaled BEOL interconnects is the elimination of the bottom diffusion barrier layer, which contributes significantly to overall device resistance [8,9]. Removing the bottom barrier layer directly increases the effective metal cross-section and reduces resistive losses, offering a meaningful improvement in interconnect performance [8,9]. Additionally, removal of the bottom barrier reduces interface complexity and may improve overall process yield by avoiding defect prone barrier-metal interfaces. This integration scheme can be enabled through area-selective atomic layer deposition (AS-ALD), a technique that allows material deposition only on desired surfaces by leveraging differences in local surface chemistry [10,11]. AS-ALD has emerged as a promising approach for extending Cu interconnect technology while preserving existing materials and process flows [8,9,12]. Unlike conventional blanket deposition approaches, AS-ALD provides intrinsic selectivity, enabling precise control over where films nucleate and grow [13]. While area-selective deposition using physical vapor deposition (PVD) typically results in non-conformal films and therefore necessitates thicker layers to achieve complete coverage, the combination of area selectivity with atomic layer deposition (ALD) offers a distinct advantage [10,12,14]. ALD inherently yields highly conformal films with precise thickness control, even within high-aspect-ratio features [9,12]. When implemented successfully, AS-ALD enables the growth of ultra-thin, fully conformal films only on targeted surfaces, thereby minimizing parasitic material volume. Depositing exclusively on targeted surfaces, AS-ALD further provides a bottom-up pathway for precise barrier and liner engineering. This capability then enables direct metal-on-metal (MoM) deposition, wherein barrier or liner materials are selectively retained on the sidewalls while being eliminated at the bottom of the interconnect trench. Overall, selective barrier elimination enabled by AS-ALD represents a compelling strategy to extend copper interconnect technology. By reducing line resistance, simplifying integration complexity, and maintaining compatibility with existing BEOL process flows, this approach offers an adaptable solution for continued interconnect scaling at advanced technology nodes.

Conventional metrology on blanket areas primarily focuses on average film thickness, uniformity, and composition, typically inferred from elemental signal intensities [15,16,17]. In contrast, AS-ALD on patterned structures requires quantification of differential growth behavior between adjacent regions, specifically distinguishing growth from non-growth surfaces. Metrology must therefore resolve film deposition on intended versus unintended surfaces, thickness differences on the order of angstroms and partial or imperfect selectivity. AS-ALD processes often rely on self-assembled monolayers (SAMs) or other surface treatments that are only a few angstroms thick. These layers may not introduce new elemental species and can be chemically similar to surrounding dielectrics, resulting in signals that are indistinguishable in raw elemental spectra. Consequently, metrology must be pattern-aware and capable of resolving signals from chemically and spatially adjacent materials within densely patterned features. Previous studies of area-selective deposition (ASD) processes using inline techniques like X-ray photoelectron spectroscopy (XPS), scatterometry, and atomic force microscopy (AFM) have primarily been conducted on blanket substrates or patterned structures with relatively large pitch dimensions and compositionally distinct surfaces [18,19,20]. As device dimensions continue to shrink at advanced logic nodes, inline, surface sensitive, and non-destructive metrology becomes essential for effective process development and manufacturing control. This places strong emphasis on techniques such as XPS, augmented with novel analytical approaches designed to resolve spectral responses from patterned structures and enable rapid actionable feedback [21]. This work demonstrates the application of inline XPS to monitor AS-ALD processes on sub 3nm BEOL Cu line space patterned structures. A wide range of line-space designs is included to study the behavior of area-selective processes across varying pattern densities. Advanced analytical algorithms are developed to extract surface specific barrier liner growth thicknesses and material specific inhibitor signatures from overlapping spectral features, enabling quantitative assessment of selectivity on densely patterned interconnect structures.

2. PROCESS DEVELOPMENT AND METROLOGY

Integration of ASD into BEOL processing for bottomless barrier applications can significantly enhance device performance. The ASD process sequence begins with the formation of the bottom metal line (Figure 1a), followed by deposition of a self-assembled monolayer (SAM) (Figure 1b). The SAM, composed of organic molecules designed to spontaneously assemble on a metal surface only, acts as an inhibitor for subsequent AS-ALD barrier deposition. The quality and completeness of the SAM directly determine the effectiveness of barrier inhibition. A critical requirement for maintaining SAM integrity is preventing any air exposure between SAM formation and TaN deposition. Prior studies have shown that even brief exposure to ambient environments can lead to SAM degradation and loss of selectivity on blanket wafers [12]. As a result, SAM characterization is typically limited to sister wafer analysis or measurements at early process development stages. Direct SAM measurement is also challenging because the organic SAM signal usually overlaps strongly with that of BEOL dielectric materials. Once SAM is deposited, multiple AS-ALD growth cycles of barrier liner are enabled to achieve desired thickness on the unprotected dielectric areas (Figure 1c). This results in selective growth on dielectric surfaces while suppressing deposition on metal, ultimately enabling metal on metal contact without a bottom barrier (Figure 1d). A key challenge, however, is how to measure and monitor these process steps inline. The metal line dimensions are about a few tens of nanometers, while the growth layer thicknesses are only a few angstroms to a couple of nanometers. Therefore, any metrology technique to monitor and measure these processes must be in-line, non-destructive, surface sensitive, capable of resolving angstrom level film thicknesses, and be able to measure patterned metrology targets with a sufficiently small spot size. XPS meets these requirements and can be implemented in-line with small spot size capability. XPS is based on the photoelectric effect, meaning when the sample is irradiated with monochromatic X-rays, atoms absorb photons and undergo photoionization, emitting core-level electrons and creating a vacancy. The emitted electrons travel through the material and can escape into vacuum, where they are collected by an energy analyzer. The detector counts the number of electrons at each energy window. When the photon energy exceeds the electron binding energy, the electron is emitted with the remaining kinetic energy, enabling identification of elemental composition and chemical state with angstrom level sensitivity [15,16,17].

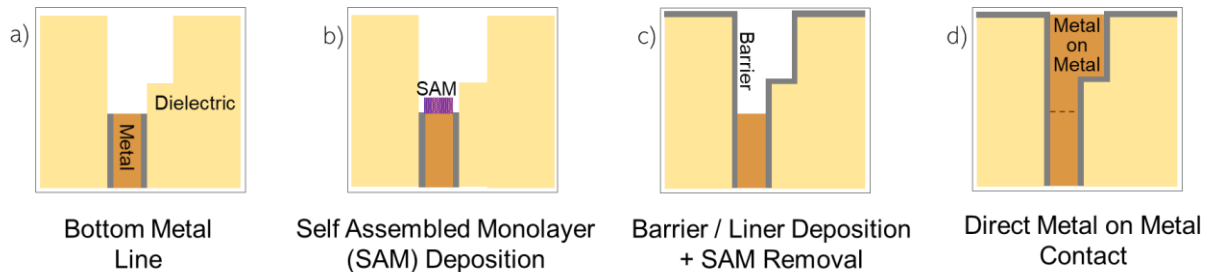


Figure 1. Schematic of area-selective atomic layer deposition processes on BEOL Cu line space structures for metal-on-metal integration (a) bottom metal structure; (b) post SAM formation on desired metal surface; (c) post barrier liner growth on desired dielectric surface; (d) metal-on-metal formation.

For un-patterned single layer or multi-layer films, layer thicknesses can be determined directly using peak fit extracted signal intensities from the measured raw XPS spectra, effective attenuation lengths which is a function of electron escape depths, absorption constants and attenuation of substrate photoelectron signals through an overlayer using the Beer-Lambert relationship [15,16,17,21]. However, with patterning, traditional XPS solutions are not sufficient. In patterned geometries, elemental intensities are strongly influenced by structural factors such as line width and pitch, and volumetric distribution of contributing materials (Figure 2a). Additionally, many BEOL dielectric elements may be chemically identical to elements present in the growth elements, making them indistinguishable in the raw spectra. For example, accurate SAM quantification requires separating the SAM related signal from any identical elemental contributions originating from dielectric layer. Ideally, SAM is desired to grow only on Cu surface to inhibit barrier growth and barrier liner is desired to grow exclusively on the dielectric area. However, deviations from nominal process conditions can lead to growth occurring on unintended regions, further complicating spectral interpretation (Figure 2b, Figure 2c). Considering all these challenges, analyzing patterned structures requires complex data interpretation that extends well beyond standard 1D film stack analysis. XPS measurements on 2D and 3D patterned structures must incorporate advanced modeling

approaches that account for geometry dependent intensity scaling and a data feed-forward framework that integrates structural information from prior measurement steps. Such methods are essential for accurately resolving ultrathin films and distinguishing growth on desired versus undesired surfaces in area-selective deposition processes.

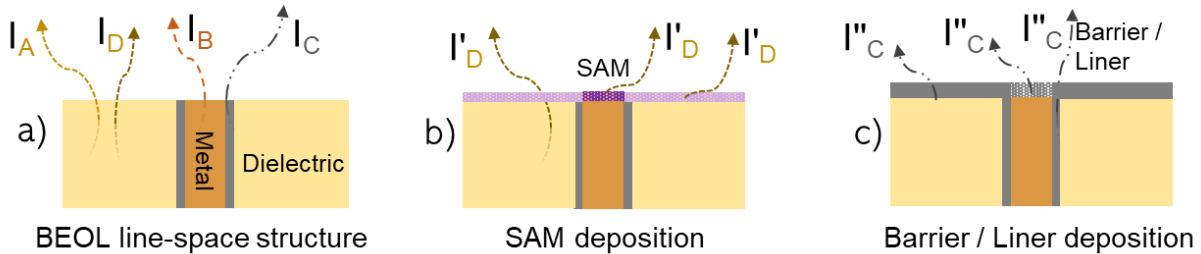


Figure 2. Schematic of Cu line-space structures showing contributions of XPS elemental intensities from different materials in the structure (a) elemental intensities from Cu (I_B), liner (I_C) and dielectric (I_A & I_D) layers post Cu CMP process; (b) elemental intensities from dielectric layer (I'_D), desired SAM layer (I''_D) on metal surface and undesired SAM layer (I'_D) on dielectric surface post surface inhibitor deposition; (c) elemental intensities from barrier layer (I''_C) post barrier layer deposition on desired dielectric surface and undesired metal surface.

For this work, we have developed models to measure ASD processes using an inline XPS system (Nova Veraflex IV) and its advanced algorithms. These advanced algorithms take into consideration unique elemental intensity ratios (I_A , I_B , I_C and I_D) from the measurement target before any material growth happens, which forms structure correction factor (g_A) (Figure 3a). This structure correction factor (g_A) is critical because it encodes the elemental intensity contributions from the underlying structure prior to any growth or deposition occurs. Since the underlying structure remains unchanged throughout the subsequent deposition steps, any variation in measured intensity can be attributed solely to the growth layers. This structural information is fed forward into subsequent analysis steps in the form of measured intensity ratios (Figure 3). For example, post barrier deposition (Figure 3c), the dielectric layer intensity is attenuated (I''_C) by the intended barrier liner growth of thickness t_{c1} on the dielectric surface. Similarly, the metal layer intensity is attenuated (I''_B) by the non-intended growth of barrier liner of thickness t_{c2} on metal surface. For an ideal selective deposition process, the metal surface should exhibit no barrier nucleation, resulting in no measurable change in the metal XPS intensity. By evaluating the structural intensity information from the pre-deposition measurement structure, the attenuation ratios of both the metal and dielectric intensities along with the measured barrier liner intensity at the post barrier deposition step, growth on both desired and undesired surfaces can be characterized. In situations where the elemental signatures of the deposited film and the BEOL dielectrics overlap, integrating this information into the structure correction factor (g_A) allows the model to resolve the growth contributions with high accuracy (Figure 3b).

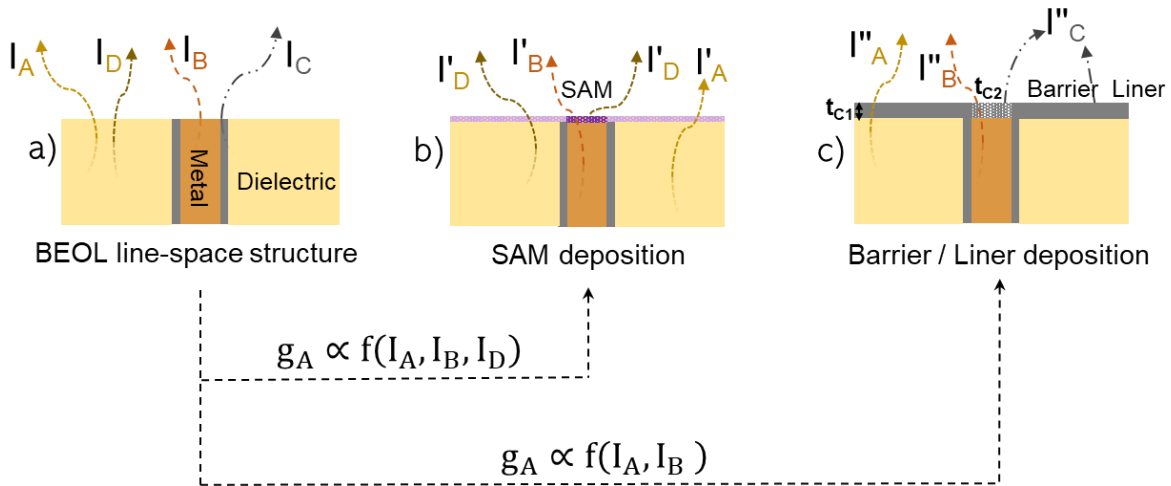


Figure 3. Schematic of Cu line-space structures illustrating XPS elemental signal contributions and structure factor feed forward analysis (a) elemental intensities from Cu (I_B), liner (I_C) and dielectric (I_A & I_D) layers post Cu CMP process; (b) SAM analysis using structure correction factor (g_A) along with elemental intensities from Cu (I'_B), dielectric (I'_A & I'_D) and SAM (I'_D) layers ; (c) Barrier growth analysis using structure correction factor (g_A) along with elemental intensities from Cu (I''_B), dielectric (I''_A & I''_D) and barrier liner (I''_C) layers.

3. DESIGN OF EXPERIMENTS

To evaluate the applicability and sensitivity of advanced in-line XPS in analyzing bottomless barrier deposition flows, a systematic study was conducted using patterned Cu line-space structures spanning a range of line widths and pitches fabricated on 300 mm Si wafers. These Cu lines were processed at the backend Mx level. The nominal line-width information, along with the line-to-pitch ratios, are listed in Table 1. The targets encompass blanket dielectric (T1) and metal (T11) pads, along with patterned structures containing metal line widths from 1x to 10x and multiple line-to-pitch density configurations (T2 – T10).

Table 1. List of BEOL measurement targets designed and analyzed in this work.

Target #	Metal line width (a.u)	Metal line to pitch (%)
T1	Dielectric Pad	0
T2	1x	14.9
T3	1x	30.4
T4	1x	38.9
T5	1x	50
T6	1.3x	50
T7	2.6x	50
T8	2x	58.3
T9	4x	73.7
T10	10x	85.4
T11	Metal Pad	100

XPS spectra were acquired immediately following the Cu CMP process (Figure 4a) to provide the pre-deposition reference, capturing elemental intensities prior to the introduction of any subsequent growth layers.

3.1 Process A

A set of wafers were sequentially processed through the surface pre-clean step (Figure 4b), SAM deposition (Figure 4c), and TaN barrier deposition steps (Figure 4d), as illustrated in Figure 4. Optimal process conditions for achieving highly selective TaN growth favoring preferential deposition on dielectric surfaces while suppressing growth on Cu surfaces, were attained through careful control of surface preparation and deposition sequence. The wafer surface was cleaned prior to SAM deposition to remove any contaminants or native oxides, and the subsequent TaN layer was immediately deposited in-situ without exposing the SAM coated surface to ambient air to enable maximum selectivity.

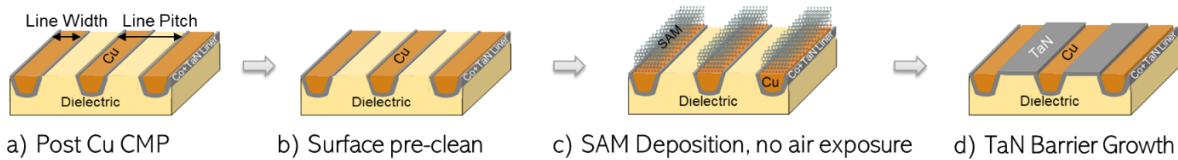


Figure 4. Schematic of area-selective atomic layer deposition processes on BEOL Cu line space structures: Measurement structures (a) post Cu CMP process; (b) post surface pre-clean; (c) post SAM growth with no air exposure; (d) post TaN deposition.

3.2 Process B

To identify and characterize deviations from ideal process conditions, a series of controlled experiments were conducted (Table 2). The surface pre-clean step was intentionally omitted prior to SAM deposition (Table 2(B1)) to enable a systematic evaluation of surface quality influence on SAM formation and subsequent TaN selectivity. Additional experiments were performed in which the SAM coated wafers were deliberately exposed to ambient air. This allows to isolate and quantify the impact of air induced degradation such as moisture uptake or partial monolayer desorption on SAM quality and its ability to suppress TaN nucleation on Cu surfaces (Table 2(B2) and Table 2(B3)). Together, these process deviations provided a comprehensive framework for understanding the influence of SAM and its sensitivity to upstream selective TaN deposition.

Table 2. Schematic representations of key process deviations from ideal conditions considered in this study.

Process condition	Surface pre-clean	SAM deposition	Air exposure	TaN deposition
B1: Skip surface pre-clean process condition	No	Yes	No	Yes
	(a)	(b)	(c)	(d)
B2: Air exposed SAM process condition	Yes	Yes	Yes	Yes
	(a)	(b)	(c)	(d)
B3: Skip surface pre-clean and air exposed SAM process condition	No	Yes	Yes	Yes
	(a)	(b)	(c)	(d)

3.3 Process C

For this study, a set of wafers without any SAM deposition were also processed (Figure 5). These wafers provided additional reference for understanding intrinsic TaN nucleation behavior on both Cu and dielectric surfaces in the absence of surface-blocking chemistry. In the absence of a SAM layer, TaN nucleates according to the inherent surface chemistry of Cu and the surrounding dielectrics. Without any molecular blocking effects, this TaN baseline on individual surfaces allows for direct comparison of inherent growth behavior against process driven variations. In effect, these wafers established the reference point needed to evaluate the true contribution of TaN growth and calibrate our XPS algorithms.

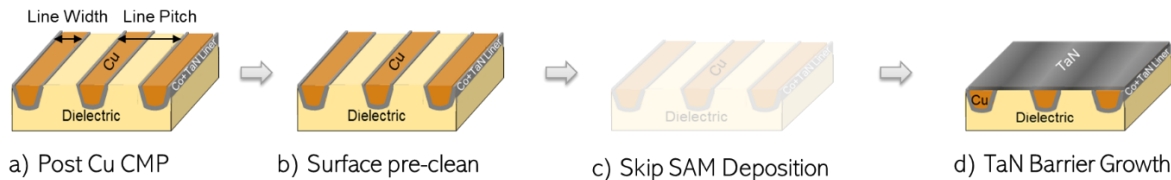


Figure 5. Schematic of area-selective atomic layer deposition processes on BEOL Cu line space structures: Measurement structures (a) post Cu CMP process; (b) post surface pre-clean; (c) skip SAM deposition; (d) post TaN deposition.

To further evaluate measurement robustness, SAM and TaN deposition cycles were also varied to assess the sensitivity of the inline XPS measurements to differences in film growth and to verify that the analysis algorithms could reliably resolve thickness changes across a broad range of deposition conditions.

4. RESULTS AND DISCUSSION

SAM and TaN growth were measured and analyzed for all previously described process variations using inline XPS combined with advanced algorithms. Clear distinctions emerged across the process splits. Nominal condition (process A) exhibited near perfect selectivity for both SAM growth and TaN growth. In contrast, deviations from ideal processing in process conditions B and C resulted in minimal to complete loss of TaN selectivity.

4.1 XPS Post TaN Deposition (Nominal process with SAM)

Selectivity was maximized when the Cu surface underwent a dedicated pre-clean immediately prior to SAM deposition, ensuring removal of native oxides and adventitious contaminants that would otherwise inhibit SAM formation or create unintended nucleation sites. Following SAM deposition, the transition to TaN deposition without any exposure of the SAM-modified surface to ambient atmosphere proved critical. Maintaining an in-situ environment prevented moisture uptake, oxidation, and partial SAM desorption, all of which are known to compromise the integrity and blocking capability of organic monolayers. Under these optimized conditions, the SAM layer remained chemically intact and functionally robust during the subsequent TaN process, enabling clear differentiation between Cu and dielectric surfaces and supporting consistent, reproducible selective barrier growth across the wafer (Process A, Figure 4, Figure 6a). The plot in Figure 6b summarizes the TaN thickness from all measurement targets extracted separately on Cu and dielectric surfaces. On the dielectric surfaces, the measured TaN thickness for 1x TaN deposition cycles closely matches the expected layer growth values. In contrast, the corresponding TaN thickness on Cu remains at or near zero across all structures, with values far below the selectivity failure threshold limit defined for achieving optimum bottomless-barrier integration scheme. This threshold value serves as a quantitative indicator of surface selectivity, exceeding it would signify a breakdown in TaN growth suppression on Cu surfaces. The minor pattern-density dependence is consistent with local surface chemistry variations observed in SAM thickness results.

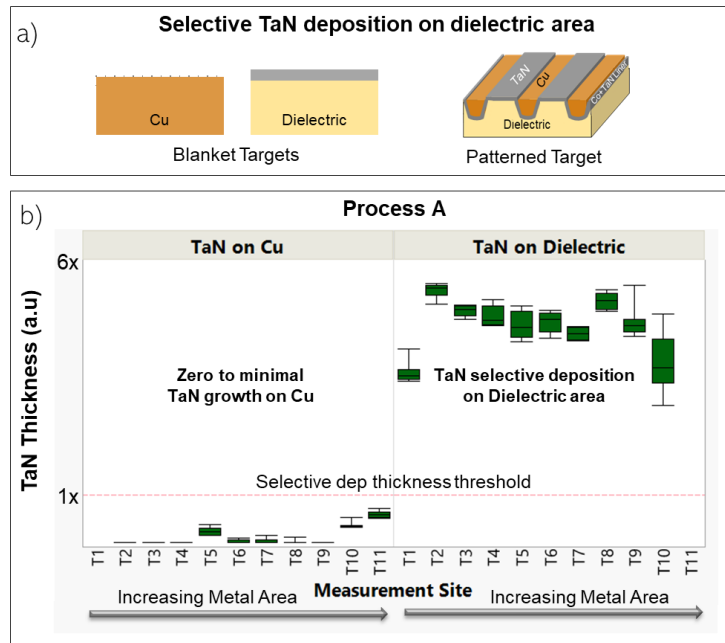


Figure 6. (a) Schematic of TaN deposition on blanket and patterned structures with nominal area-selective process condition; (b) TaN XPS thickness results calculated across all targets shown separately on Cu and dielectric surfaces.

The XPS raw spectra in Figure 7a further support this interpretation. TaN signal intensity increases monotonically with increasing dielectric fraction, indicating that measurable TaN growth is restricted to the dielectric regions. Importantly, this pattern density effect appears only when the deposition process is area-selective. In a non-selective regime, all line-space targets would exhibit near similar TaN intensity levels regardless of pattern density. To independently validate the spatial distribution of the film, EDX mapping was performed for two extreme line width patterned targets (T2 and T10) as shown in Figure 7b. In both cases, the maps corroborate XPS results, confirming that TaN nucleation occurs exclusively on dielectric surfaces and affirming the selective nucleation behavior.

An additional experiment was conducted to evaluate whether increasing SAM exposure enhances selectivity. Doubling the SAM deposition time produced no measurable change in TaN thickness or TaN selectivity (Figure 8). This behavior is consistent with the self-limiting nature of SAM formation and once a saturated monolayer is achieved, additional precursor dose did not increase coverage or modify selectivity performance.

Collectively, these results demonstrate that Process A meets the key requirements for area-selective TaN deposition, achieving robust suppression on Cu and predictable, pattern-dependent growth on dielectric surfaces.

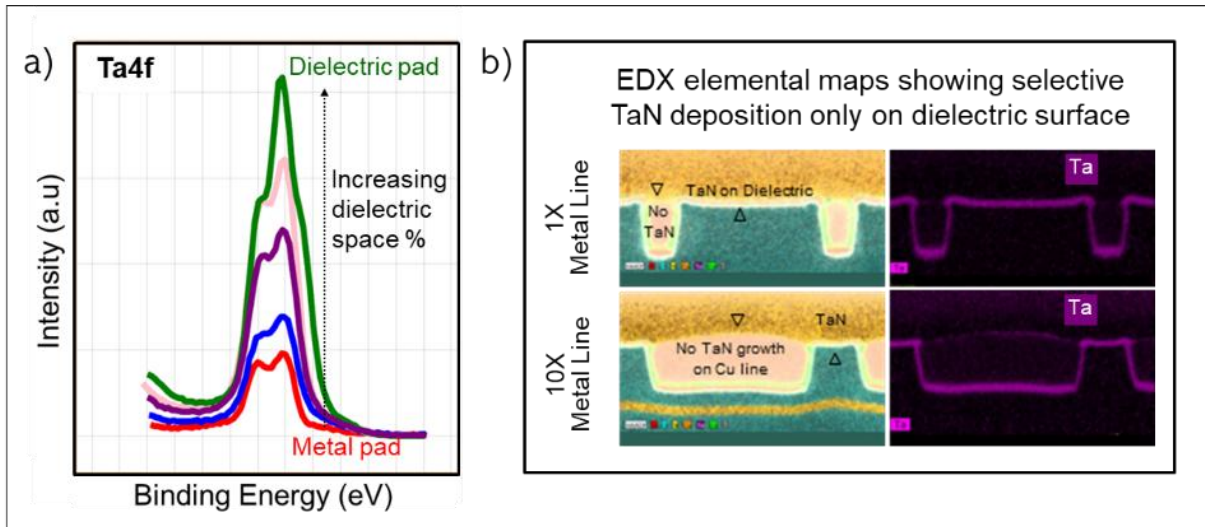


Figure 7. (a) XPS spectra on Ta for a subset of measurement targets; (b) EDX maps of measurement targets T2 (1x metal line) and T10 (10x metal line) showing exclusive TaN growth on dielectric surfaces.

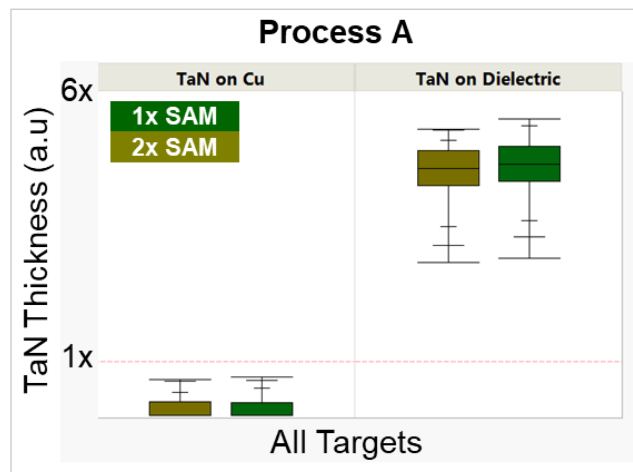


Figure 8. Consolidated TaN XPS thickness results calculated across all targets shown separately on Cu and dielectric surfaces with two different SAM deposition cycles.

4.2 XPS Post TaN Deposition (Skip SAM condition)

In the absence of a SAM blocking layer, TaN is expected to nucleate and grow uniformly across all surfaces (Process C, Figure 5, Figure 9a). Consistent with this expectation, TaN thickness measurements resolved separately on Cu and dielectric regions across the metal pad, dielectric pad, and patterned line-space targets demonstrate clear measurable TaN growth on both surface types (Figure 9c). Data analyzed from two different TaN ALD cycle counts further validated the expected deposition behavior, showing a proportional increase in TaN thickness with increase in the number of ALD cycles. Notably, the experiment also revealed that TaN growth is inherently non-uniform between Cu and dielectric surfaces, an asymmetry that is clearly reflected in the raw spectral data on Cu pad vs dielectric pad (Figure 9b). These observations indicate that the underlying surface chemistry and surface characteristics strongly influence TaN nucleation behavior even in the absence of SAM. The TaN only samples therefore served not only as a baseline for understanding intrinsic growth tendencies, but also as critical references for calibrating our analytical algorithms and validating thickness extraction from the raw TaN XPS spectra.

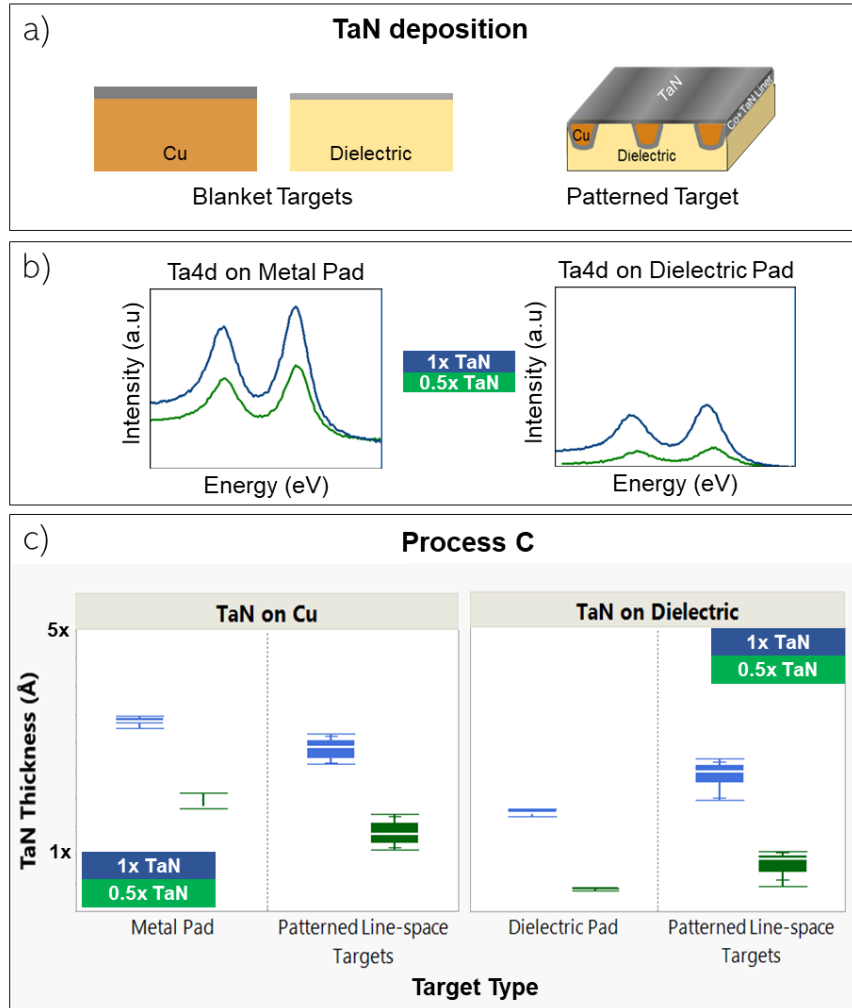


Figure 9. (a) Schematic of TaN deposition on blanket and patterned structures with skip SAM condition; (b) Ta4d XPS spectra comparison on metal pad and dielectric pad; (c) TaN XPS thickness results calculated across all targets shown separately on Cu surface and dielectric surfaces for two different TaN deposition conditions.

4.3 XPS Post TaN Deposition (Skip pre-clean / air exposed SAM process conditions)

In contrast to the nominal selective deposition behavior observed in Process A, various deviations introduced in Process B exhibit clear signatures of selectivity loss. When the surface pre-clean step was intentionally omitted (Table 2(B1)), the TaN thickness for 1x deposition cycles measured on the undesired growth region (Cu) drifted toward, and in some cases exceeded, the selective deposition threshold (Figure 10). This loss in suppression indicates that eliminating the pre-clean adversely affects SAM quality, thereby weakening its ability to inhibit TaN nucleation on Cu.

A second condition within Process B involved exposing SAM-coated wafers to ambient air prior to TaN deposition (Table 2(B2)). In this case, the TaN thickness for 1x deposition cycles on Cu surface increased well above the acceptable selectivity threshold (Figure 11a). This behavior is consistent with SAM degradation or partial desorption upon air exposure, which reduces its passivation efficiency and enables nucleation on the metal surface. To further validate the XPS extracted results, the experiment was repeated with varying TaN deposition cycles. The measured TaN thickness scaled proportionally with the number of cycles (Figure 11a), confirming that the observed trends are reliable and process driven. Complementary EDX mapping for 1x TaN deposition cycles (Figure 11b) further supported these results. For the air-exposed wafers, the EDX maps on Targets T2 & T10 clearly revealed TaN present on both Cu and dielectric regions, demonstrating a loss of surface selectivity due to to SAN quality degradation.

Overall, these results demonstrate that XPS not only captures the intended selective behavior under nominal conditions but also detects deviations arising from incomplete SAM formation or environmental exposure with required sensitivity.

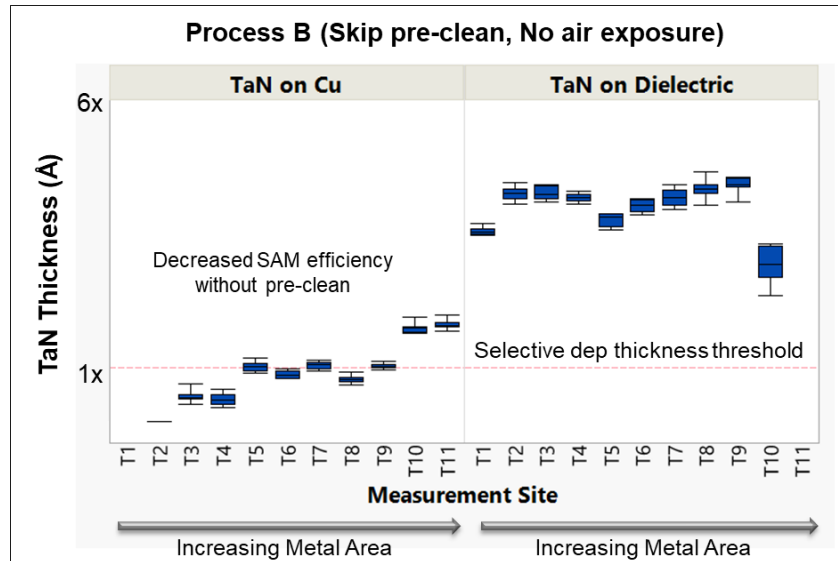


Figure 10. TaN XPS thickness results on Cu and dielectric surfaces showing slight loss in selectivity due to decreased SAM efficiency for skip pre-clean condition.

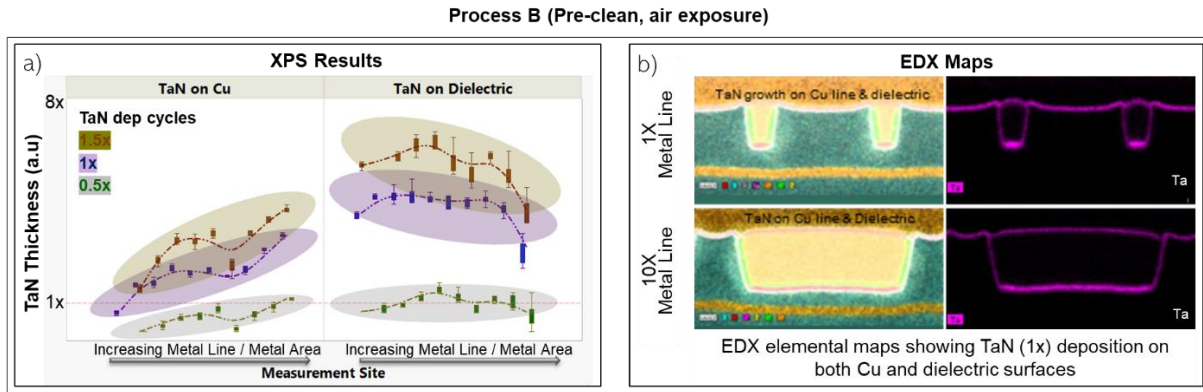


Figure 11. (a) TaN XPS thickness results across varying ALD growth cycles on Cu and dielectric surfaces showing complete loss of selectivity resulting from SAM degradation; (b) EDX maps of measurement targets T2 (1x metal line) and T10 (10x metal line) showing TaN growth on both Cu metal and dielectric surfaces.

XPS measurements were also collected after SAM deposition to quantify SAM thickness on both desired Cu and undesired dielectric surfaces. Direct monitoring of SAM growth requires careful accounting of carbon originating from the dielectric itself, when carbon is present in its composition. In our samples, the backend dielectric stack includes materials that contain intrinsic carbon, which contributes to a background carbon signal independent of any SAM coverage (Figure 12a). Without including dielectric only carbon from the pre-SAM measurement target as a distinct parameter in the structure factor, SAM specific carbon intensity cannot be distinguished from the dielectric background (Figure 12b). By applying a feed-forward methodology together with advanced analytical models capable of separating SAM derived carbon from dielectric originating carbon, reliable extraction of SAM thickness was achieved. Because the SAM quality is known to degrade rapidly upon ambient air exposure, sister wafers were intentionally exposed to air to quantify the SAM thickness, while the primary wafers proceeded directly to TaN deposition without any air break. Figure 15c presents results from one of

these air exposed wafers with skipped pre-clean step (Process B, Table 2(B3)). The skip-clean condition was chosen to enable accurate analysis by preventing unintentional loss of surface signal due to potential material removal during the pre-clean step, while also preserving the native surface state to maximize metrology fidelity. When plotted across all patterned structures (T2 – T10), the data consistently confirm selective SAM formation only on Cu surfaces (Figure 12c). The observed pattern density dependent thickness variation could be attributed to variations or irregularities in local surface chemistry across certain patterned features.

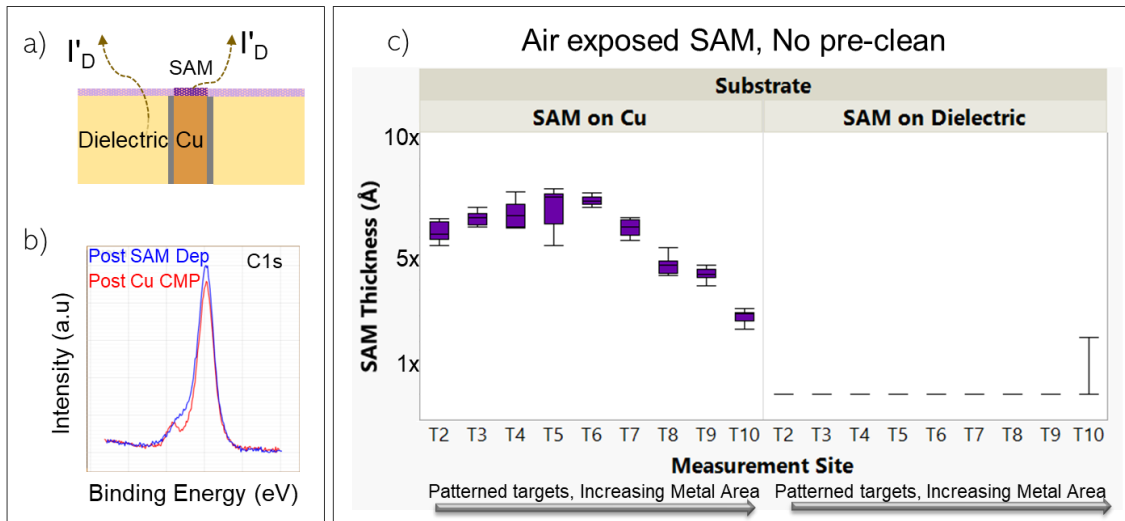


Figure 12. (a) schematic of identical elemental intensities detected using XPS from a Cu line space structure post SAM growth; (b) XPS carbon (C1s) spectra collected after Cu CMP and after SAM deposition; (c) SAM XPS thickness results shown separately on Cu and dielectric surfaces

4.4 TaN Selectivity (All process conditions)

Selectivity can be quantified through several approaches [20,22]. In this study, we adopted a thickness based metric that uses the measured TaN thickness on both the desired growth region (dielectric surface) and the undesired growth region (Cu surface) to construct a thickness based selectivity indicator. We compute the fractional contribution of each surface by comparing the TaN thickness on that surface to the total TaN deposited across both regions as shown in Figure 13a. This normalization provides a direct measure of how strongly each surface participates in the deposition process. Figure 13b presents the resulting selectivity parameter, expressed as the fraction of total deposited TaN residing on the dielectric surface. A selectivity value of 1 corresponds to ideal behavior with TaN deposited solely on the dielectric, with complete suppression on the Cu surface. A value of 0.5 indicates equal film accumulation on Cu and dielectric.

Under the nominal selective deposition condition Process A, the line-space structures exhibit selectivity values of 1 or approaching 1, confirming near-perfect preferential growth on the dielectric regions. When the pre-clean is skipped before SAM deposition or when SAM coated wafers were intentionally exposed to ambient air in Process B conditions, the selectivity ratio decreased considerably. This reduction is consistent with SAM degradation, which diminishes its ability to inhibit TaN nucleation on Cu. In the absence of SAM in Process C condition, the selectivity drops even further, falling below 0.5, indicating non-uniform TaN nucleation driven by the intrinsic differences between unpassivated Cu and dielectric surfaces.

The selectivity metric provides a sensitive and quantitative means of identifying the process window for robust selective deposition. It also reveals the cycle limits at which SAM based inhibition begins to deteriorate and provides information that is essential for evaluating the viability of area-selective TaN deposition in advanced nanoscale patterning schemes.

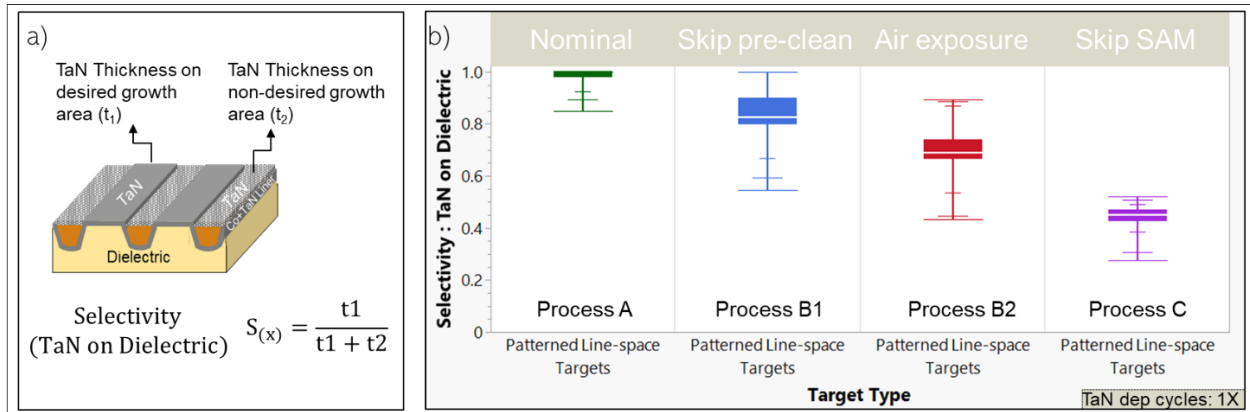


Figure 13. (a) Surface selectivity estimation using fractional growth on individual surfaces; (b) Selectivity of TaN on dielectric surface across all patterned targets for various process conditions

5. CONCLUSIONS

This paper explored interconnect scaling challenges and discussed bottomless barriers enabled by area-selective atomic layer deposition as a viable potential solution to extend Cu interconnect technology. We presented an inline metrology framework for characterizing and monitoring back-end AS-ALD processes using advanced XPS based analysis algorithms tailored for patterned structures. The solutions developed can be used to deconvolute growth elements from back-end dielectrics. These novel algorithms were able to accurately measure growth layers SAM and TaN thickness results on both desired and non-desired growth areas on patterned targets. With our experiments on a wide design space, the models were shown to not only measure and monitor nominal processes but were also shown to capture all other failure modes that can occur in manufacturing line. The results were validated with EDX map analysis and showed excellent correlation to process trends. The methods discussed here have potential to expand to direct device level measurements, integrated via structure measurements, to any other emerging alternate back-end materials and hybrid metrology approaches that combine OCD and XPS techniques.

6. ACKNOWLEDGEMENTS

The authors would like to thank IBM management for supporting this work. They would also like to thank IBM colleagues Connor Franzese, Shorna Hamilton, Asef Nazari and Chris J. Penny from the Patterning and Metrology team for their assistance with the experimental runs, and colleagues from the Failure Analysis Laboratory for their support with EDX measurements. The authors further acknowledge Larry Bot, Igor Turovets, Avron Ger and Shay Wolfling from Nova for their support in this work.

REFERENCES

- [1] G. Bonilla, N. Lanzillo, C.-K. Hu, C. J. Penny, and A. Kumar, "Interconnect scaling challenges and opportunities to enable system-level performance beyond 30 nm pitch," in Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), 2020, doi: 10.1109/IEDM13553.2020.9372093.
- [2] K. Motoyama, "Advanced Interconnect Technologies for Cu Extension and Beyond," in Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2025.
- [3] International Technology Roadmap for Semiconductors (ITRS), "Interconnect," ITRS 2013 Edition, Semiconductor Industry Association, 2013.
- [4] J. H. Moon, E. Jeong, S. Kim, T. Kim, E. Oh, K. Lee, H. Han, and Y. K. Kim, "Materials quest for advanced interconnect metallization in integrated circuits," *Advanced Science*, vol. 10, no. 23, Art. no. 2207321, Jun. 2023, doi: 10.1002/advs.202207321.

- [5] M. J. M. Merckx and A. J. M. Mackus, "Area-selective ALD of diffusion barriers for via optimization – There is plenty of room at the bottom," *Atomic Limits*, vol. 7, 2022.
- [6] J. H.-C. Chen, N. LiCausi, E. T. Ryan, T. E. Standaert, and G. Bonilla, "Interconnect performance and scaling strategy at the 5 nm node," *Proc. IEEE Int. Interconnect Technology Conf., Adv. Metallization Conf., IITC/AMC*, 2016, pp. 12–14
- [7] D. Edelstein, A. Jog, S. Nguyen, H. Huang, S. Ghosh, S. Choi, N. Lanzillo, M. Lofaro, S. McDermott, D. Metzler, Y. Mignot, T. Nogami, F. Petrescu, M. Shoudy, M. Silvestre, A. Simon, L. Wangoh, H. Zhang, and K. Choi, "Innovations enabling the continued extendibility of Cu and post-Cu damascene BEOL technologies, Proceedings of the 2025 IEEE International Interconnect Technology Conference (IITC), 2025 doi: 10.1109/IITC66087.2025.11075366.
- [8] J. Jang, K. Park, C. Park, S. Yoo, S. Cha, K. Nam, K. Kim, J. Son, E. Park, J. Lee, J. Kim, M. Lee, M. Yeo, E. Jung, R.-H. Kim, D. Park, C. Kim, Y. Choi, T. Ha, J. Ahn, and J. Ku, "Extremely advanced Cu interconnect with selective ALD barrier for high-performance logic device," in *Proceedings of the IEEE International Interconnect Technology Conference / Materials and Metallization (IITC/MAM)*, 2023, doi: 10.1109/IITC/MAM57687.2023.10154689.
- [9] S. You, H. Ren, M. Naik, L. Chen, F. Chen, C. Leal Cervantes, X. Xie, and K. Kashefzadeh, "Selective barrier for Cu interconnect extension in 3 nm node and beyond," in *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, 2021, doi: 10.1109/IITC51362.2021.9537559.
- [10] K. Lioni, N. Arellano, N. Lanzillo, S. Nguyen, P. S. Bhosale, H. Bui, T. Topuria, and R. J. Wojtecki, "Area-selective deposition of tantalum nitride with polymerizable monolayers: From liquid to vapor phase inhibitors," *Chemistry of Materials*, vol. 34, no. 7, pp. 2919–2930, 2022, doi: 10.1021/acs.chemmater.1c03436.
- [11] R. Wojtecki, M. Mettry, N. F. Fine Nathel, A. Friz, A. De Silva, N. Arellano, and H. Shobha, "Fifteen-nanometer resolved patterns in selective area atomic layer deposition – Defectivity reduction by monolayer design," *ACS Applied Materials & Interfaces*, vol. 10, no. 45, pp. 38630–38637, 2018, doi: 10.1021/acsami.8b13896.
- [12] L. Wangoh, A. Simon, and M. Shoudy, "Optimization of area selective barrier on different metal interconnects," *Proceedings of the 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, Albany, NY, USA, 2024, pp. 1–4, doi: 10.1109/ASMC61125.2024.10545462.
- [13] A. J. M. Mackus, "Approaches and opportunities for area-selective atomic layer deposition," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, 2018.
- [14] Y. Kikuchi, M. Iwashita, H. Nagai, H. Komatsu, Y. Ozaki, K. Fujita, G. Pattanaik, H. Kawasaki, and K. Iwai, "Performance improvement for Cu interconnects by SAM and ELD technologies," *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, 2022, doi: 10.1109/IITC52079.
- [15] C. R. Brundle, G. Conti, and P. Mack, "XPS and angle-resolved XPS in the semiconductor industry: Characterization and metrology control of ultra-thin films," *Journal of Electron Spectroscopy and Related Phenomena*, vol. 178–179, pp. 48–59, 2010, doi: 10.1016/j.elspec.2010.03.008.
- [16] J. F. Moulder, W. F. Stickle, P. E. Sobol, and K. D. Bomben, "Handbook of X-ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data," *Physical Electronics Division, Perkin-Elmer Corp., Eden Prairie, MN, USA*, 1992.
- [17] F. A. Stevie and C. L. Donley, "Introduction to X-ray photoelectron spectroscopy," *Journal of Vacuum Science & Technology A*, vol. 38, no. 6, Art. no. 063204, 2020, doi: 10.1116/6.0000412.
- [18] M. Krishtab, J. Hung, R. Koret, I. Turovets, K. Shah, S. Rangarajan, L. Warad, V. Zhang, R. Ameloot, and S. Armini, "Plasma-halogenated a-C:H as a growth-inhibiting layer for ASD of titanium oxide," in *Metrology, Inspection, and Process Control for Microlithography XXXIV*, *Proc. SPIE*, vol. 11325, Art. no. 113250Y, 2020, doi: 10.1117/12.2551492.
- [19] M. Saib, A. Mouss, A.-L. Charley, P. Leray, J. Hung, et al., "Scatterometry and AFM measurement combination for area-selective deposition process characterization," in *Metrology, Inspection, and Process Control for Microlithography XXXIII*, V. A. Ukraintsev and O. Adan, Eds., *Proc. SPIE*, vol. 10959, Art. no. 109591N, 2019, doi: 10.1117/12.2515177.
- [20] A. J. M. Mackus, M. J. M. Merckx, and W. M. M. Kessels, "From the bottom-up: Toward area-selective atomic layer deposition with high selectivity," *Chemistry of Materials*, vol. 31, no. 1, pp. 2–12, 2019, doi: 10.1021/acs.chemmater.8b03454.
- [21] C. J. Lee, M. Medikonda, T. McDonough, W. Parkin, R. Bao, et al., "In line XPS for advanced semiconductor manufacturing and metrology on fully integrated targets," *Proc. SPIE* 13981, 13981 7 (2026).
- [22] G. N. Parsons, "Functional model for analysis of ALD nucleation and quantification of area-selective deposition," *Journal of Vacuum Science & Technology A*, vol. 37, no. 2, Art. no. 020911, 2019, doi: 10.1116/1.5054285.