

Evaluation of inline SIMS impact on device reliability and performance

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ABSTRACT

The high-resolution compositional depth profiles generated by SIMS can provide invaluable process insights inaccessible through other techniques. Recently, inline SIMS was introduced, which embodies specific design considerations for in-fab use.¹ In this paper, possible impacts on production wafers are investigated by evaluating the potential contamination and performance-impacting defects arising from ion sputtering. Post-analysis assessments include planarization effectiveness prior to lithography, surface contamination evaluations, and electrical tests to evaluate transistor performance. It was found that craters resulting from sputtering exhibit shallow sidewall angles, allowing for effective filling by typical planarization layers coated prior to lithography with no negative impact on subsequent processing. Additionally, no evidence of surface contamination in the vicinity of the craters was observed. In-line electrical tests showed no performance or reliability impact on gate-all-around nanosheet transistors related to sputtering performed after various processing steps through front-end-of-line manufacturing. Overall, the results demonstrate that inline SIMS may be implemented as an in-line metrology solution and wafers can continue through the manufacturing line without impact on device performance.

Keywords: inline metrology, SIMS, semiconductor wafers, manufacturing, silicon, transistors

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1. INTRODUCTION

The paradigm of Moore's Law continues to shape an industry-wide roadmap towards device scaling while also driving efforts for innovative metrology that can be transferred into the high-volume manufacturing (HVM) environment and proactively solve problems without the need for offline analysis. Despite the numerous techniques that might exist in this outside domain, the time it takes for a new technique to emerge from the research stage and evolve into production readiness is about ten years.² Secondary ion mass spectrometry (SIMS) has matured as a lab-based analytical technique that has long supported advancements in semiconductor manufacturing for over 60 years. The technique offers unparalleled sensitivity for surface characterization (static operation mode) and bulk material characterization with sub ppm detection limits (dynamic operation mode). There are countless examples where SIMS in either operation mode provided key insights into semiconductor developments, including early depth profiling of shallow implants,³ contamination failure analysis,^{4,5} high-k metal gate processing,⁶ and patterning materials characterization.⁷⁻⁹ In retrospect, much of these advances can be owed to decades of advances in SIMS instrumentation,¹⁰ including magnetic sector, quadrupole, vacuum systems, time-of-flight (ToF), novel ion sources and most recently – deployment for in-line manufacturing utilization.^{1,11}

Dynamic SIMS is the latest analytical technique to transition into the fab environment in response to the high demand for a depth profiling capability to both characterize and iteratively tailor dopant distributions in S/D epitaxy used in gate-all-around (GAA) nanosheet transistors.^{12,13} In principle, the rastering action of the primary beam subsequently removes atoms from the specimen via an induced collision cascade, generating and extracting secondary ions on a layer-by-layer basis, ultimately displacing the probed volume with an open crater present on the surface. The Nova Metrion inline SIMS tool was recently outlined for its tool capabilities and highlighted applications,¹ notably as advantages over lab SIMS including fast data turnaround time (minutes), data reproducibility, simplified operation, direct feedback with processing tools, correlation with inline metrology suite, and most importantly, returning wafers back into production. However, it was

commonly believed that the SIMS tool would contaminate the surface of analyzed material due to the sputter nature, along with failed attempts to bring SIMS into a fab environment in the past.^{14,15} Primary concerns typically involve forward or back-sputtered energetic particles generated in the bombardment and ejected to flight paths at distances away from the original measurement site. Previous reports have looked into these factors including damage to sites proximal to the crater location due to neutrals from the primary beam,¹⁶ surface contamination from ion sputtering¹⁷ and impact to analyte detection limits by memory effects based on SIMS tool design.^{18,19} While omitting the need to scrap a production wafer for offline analysis is critical for process development and cost control, the wafer returned to production must not be adversely affected by inline SIMS.

Here, we performed a set of experiments to evaluate the potential production impact induced by the inline SIMS via dynamic ion sputtering and/or the open crater. As highlighted in Fig. 1, we investigated the analysis chamber for three failure modes: A) crater downstream effects B) surface sputter contamination and C) logic device contamination. To further align with such multifaceted industry demands along with stringent particle contamination requirements according to the IRDS 2023 Yield Enhancement Report,²⁰ investigation is warranted to understand how these potential degradation mechanisms that can impact production and benchmark inline SIMS as a safe metrology solution.

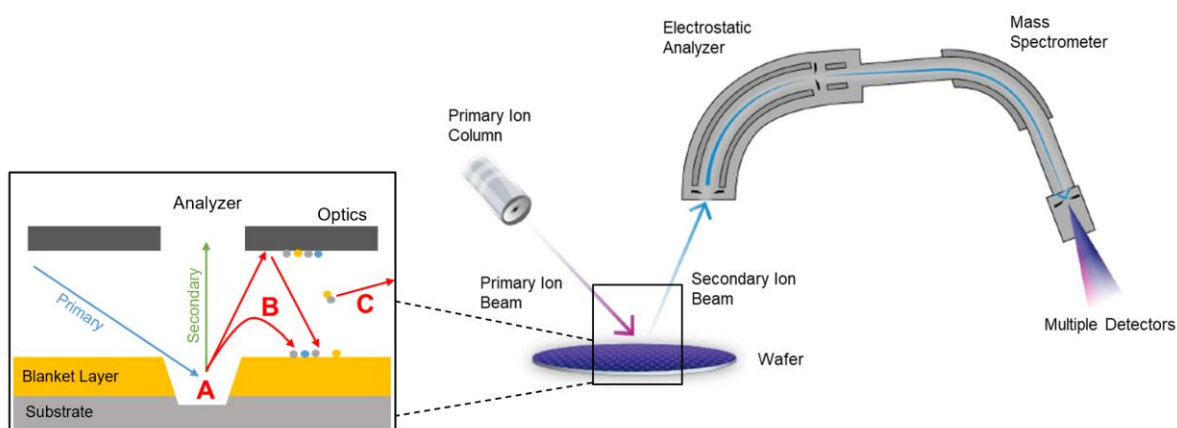


Figure 1. Schematic of the Nova Metrion inline SIMS tool components. The analysis chamber is highlighted as the focal point of investigation to evaluate three failure modes: A) crater downstream effect B) surface sputter contamination and C) logic device contamination.

2. EXPERIMENTAL DETAILS

2.1 Crater Downstream Assessment

A bare silicon wafer was routed to a process flow that includes processing through inline SIMS followed by a lithography process (Fig. 2a). For the SIMS step, a sampling map was designed to have a total of 16 craters radially generated across the wafer surface. Four beam energies (ranked nominally $A < B < C < D$) were used to generate craters with the raster area set to $50 \times 50 \mu\text{m}^2$ and depths up to 300 nm (energy A only) or up to 1000 nm (energy B, C, D) (Fig. 2b). Sputter depths and raster areas were reasonably selected considering the application space in which inline SIMS operates, production throughput, and avoiding deliberate “cratering effects” where background contributions would degrade the measured profile of an analyte as the crater is recessed deeper.²¹

The wafer bearing craters continues onto the lithography branch for a multi-level resist process, starting with the application of an underlayer stack containing an organic planarizing layer (OPL), followed by spin coating a thick resist top layer. Surface inspection measurements include an optical inspection image (WISC) using TEL Lithius ProZ for pre/post OPL step and a light scattering image (haze map) from a KLA Surfscan tool for pre/post SIMS and the post resist step.

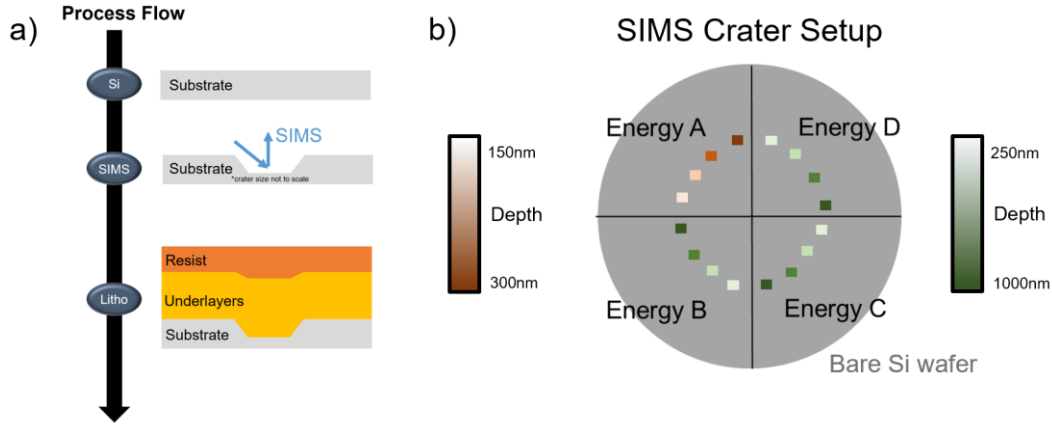


Figure 2. a) Process flow for crater downstream impact evaluation; b) Sampling plan for varied crater dimensions based on SIMS ion beam sputter parameters.

2.2 Surface Contamination Assessment

First, a blanket wafer comprised of 70 nm layer of SiGe with 35% Ge beneath a 70 nm Si layer was processed with the Nova Metrion inline SIMS tool using a single primary beam energy and a raster area of $100 \times 100 \mu\text{m}^2$. The primary beam was set to sputter through the bilayer stack and into the substrate until the Ge secondary ion signal was no longer detected, thus maximizing the full potential for ion redeposition of Ge atoms on the Si surface (Fig. 3a). Qualitative surface analysis was performed with a Nova Veraflex inline X-ray photoelectron spectroscopy (XPS) tool probing 24 multiple points on the wafer including 4 points along the underlayer sidewall and 20 points around the crater vicinity to compare the presence/absence of characteristic Ge peaks (Fig. 3b).

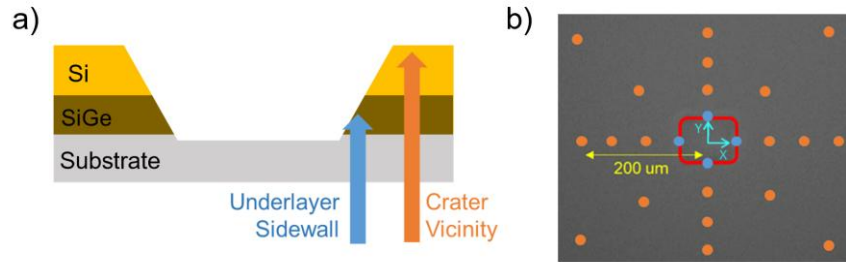


Figure 3. a) Schematic of SiGe/Si blanket stack after SIMS sputtering and highlighted probing sites of interest for XPS surface analysis; b) Sampling map for XPS measurements around the crater (red square) including 4 sites along the exposed SiGe wall (blue spots) and 20 sites for vicinal sites (orange spots).

For the second part, a blanket stack consisting of Cu buried in amorphous Si on a silicon substrate is first processed with the Nova Metrion inline SIMS tool. Three different beam energies (ranked nominally $A < B < C$) were employed to sputter the same wafer at three distinct locations along the y-axis, each sputtering over a raster area of $50 \times 50 \mu\text{m}^2$ and a depth point through the blanket stack until reaching a few nanometers into the substrate (Fig. 4a). For surface analysis, a Bruker Insight inline atomic force microscopy (AFM) tool (silicon nitride tip, nominally 2 nm tip radius, tapping mode) was used to directly measure the surface topography of three key sites on the blanket wafer: the crater bottom, crater vicinity, and a reference point set to 20 mm away from the crater. The crater was initially measured with a $120 \times 120 \mu\text{m}^2$ scan area to capture the crater and vicinal surface, along with the collection of high-resolution $20 \times 20 \mu\text{m}^2$ scan area collected at the center of the crater bottom and the reference point. To calculate roughness for each crater vicinity, the raw AFM topography images were processed using an algorithm in the AFM analysis software to smooth noise, the recessed portion

was masked to only calculate root-mean-square (RMS) using the outside area (Fig. 4b). For the crater bottom and reference sites, the full high-resolution scans area was used to calculate roughness.

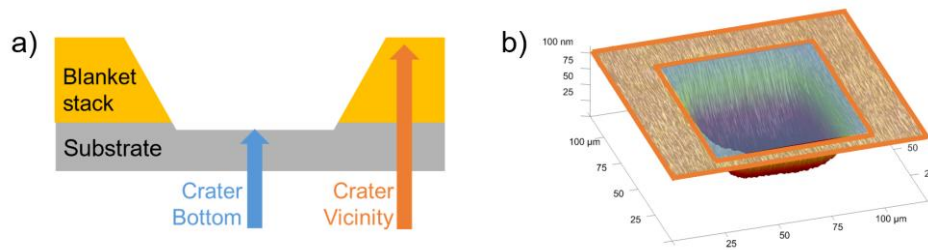


Figure 4. a) Schematic of blanket stack after SIMS measurement and highlighted probing sites on the crater for AFM surface analysis; b) Surface roughness analysis method using an example crater 3D image to demonstrate isolation of the crater vicinity (inside orange borders) from the crater walls (blue square).

2.3 Logic Device Impact Assessment

Eight production wafers designated for gate-all-around pFET test vehicle were used for this experiment – six measured with SIMS and two without SIMS – all processed from front-end-of-line (FEOL) to back-end-of-line (BEOL) route steps until reaching post M1 in-line electrical tests (Fig. 5).

Three critical FEOL steps were selected to evaluate impact due to sputter contamination: S/D epitaxy, channel release, and high-k metal gate deposition. Following completion of each FEOL process step, two wafers were split from the lot and branched pair-wise into an experimental route to process through inline SIMS, where a select N number of measurements would take place on dedicated $50 \times 50 \mu\text{m}^2$ metrology pads along the scribe of each die. For each wafer pair, one wafer received a low number of SIMS measurements and the other would receive a high number to have insight on local versus global effects that would be eminent in a 300mm production wafer exposed to such measurement conditions. Considering the increased risk for contaminating devices after channel release and high-k deposition steps, the scheme for measured dies were set to have four measurements surround a chip with tested devices for both local (1 chip, $N=4$) and global (3 chips, $N=12$) wafers. Considering these were pFET test vehicles, the exposure time (sputter time length) for each measurement was determined based on the p-dopant detected in the resulting depth profiles. This was set to maximize the potential sputter contamination of available boron dopant and all other co-ejected ions for each individual FEOL process step.

Upon completing the inline SIMS measurement step, the wafer pair was merged back with the original lot and returned to production. Once processed through M1, all wafers were tested inline for electrical performance and reliability. The two wafers not measured with inline SIMS served as control wafers (labeled Reference 1 and Reference 2) to validate the expected range for e-test results based on fab processing variability. Failure analysis was performed for further insight into outlier data points; structural and compositional characterization was performed using cross-sectional transmission electron microscopy (TEM) in conjunction with electron spectroscopy methods to map elemental distributions.

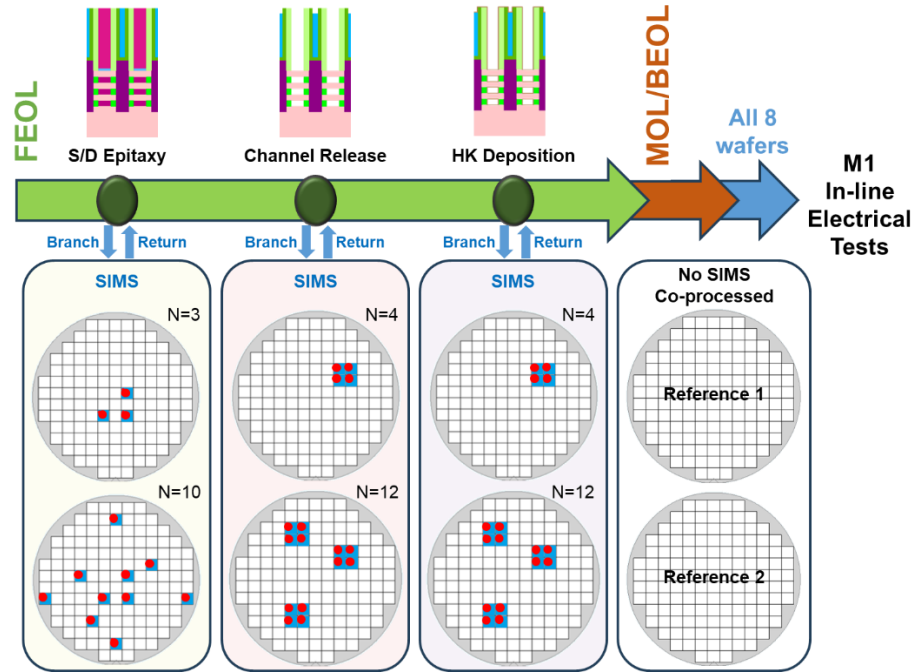


Figure 5. Schematic of device process flow and sampling plans for production wafers. Each experimental wafer had a select N number of SIMS measurements (red circles) performed on a selected set of dies (blue square).

3. RESULTS AND DISCUSSION

3.1 Crater Downstream Evaluation

Surface inspection data was used to identify a physical threshold where downstream processing defects emerge on the surface of the final lithography stack due to either severe floor topography (beam energy) or geometric dimensions (area, depth) of the SIMS crater. As suggested in Fig. 2a, it was hypothesized that a locally invasive crater could cause planarizing issues and negatively impact downstream processing of other layers in the lithography stack – resulting in the formation of comet-like defects with a head at the crater origin and a tail that would drag after spin coating the resist layer.

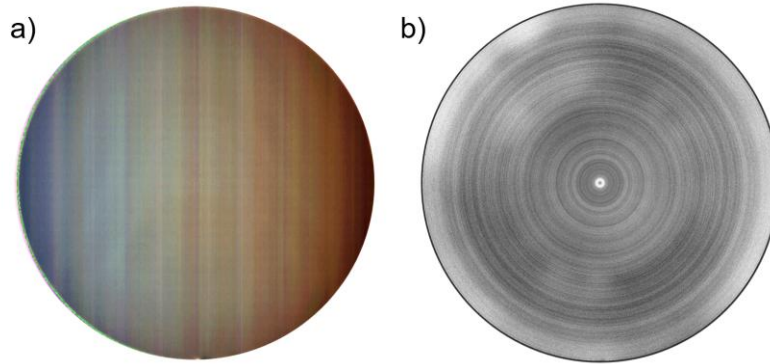


Figure 6. Surface inspection maps collected throughout the crater evaluation process flow including a) WISC image after OPL and b) haze map post resist.

WISC and haze images are generally used to assess the surface condition of patterning materials with a tight requirement on tolerable height variation, scumming, and other topographic anomalies that would impact flatness of the light-reactive surface. In the wafer maps shown in Fig. 6, no defects were observed in both the WISC and haze images collected in the respective process steps. The same experiment was also done for increased raster areas, and defects were not observed.

This observation is attributed to both the crater sidewall angles, where the maximum for these craters was about $\sim 2^\circ$ at 1000 nm of depth, as well as the relatively flat crater floor, that collectively enabled smooth and efficient planarization of all craters.

To elaborate further, SIMS ion beam sputtering will generate craters with shallow sidewall angles due to the tailing of the ion beam shape depends on the intensity Gaussian distribution that exponentially decays radially from the center to the edge of the beam.²² Energetic neutrals are inevitably generated at the edge of the focused beam, which cannot be steered due to lack of charge, and thus bombard the outer perimeter of the raster area to form sloping walls. Presence of any reactive oxygen species embedded in the substrate from the primary ion source was also not a factor impacting the planarization process. While there are engineering considerations needed for cases requiring additional treatments to clean the substrate surface or employ multiple coatings to improve the degree of planarization, the craters generated by inline SIMS did not require special precautions.²³

3.3 Surface Contamination Evaluation

The second component to qualify the inline SIMS tool is the potential redeposition of particles eroded from the solid, divert from the extraction path of the secondary beam, and land on the surface of the 300mm wafer. This is important considering the unwanted presence of particles in areas of the wafer and the effect on detection limits. Here, we are looking at 1) contamination of foreign materials on a wafer surface following SIMS sputtering and 2) physical damage to the surface from energetic particles.

XPS measurements were performed on the blanket SiGe/Si stack after SIMS sputtering through the stack and into the substrate, focusing on the $100 \times 100 \mu\text{m}^2$ crater sidewall where the SiGe layer would be exposed and the crater vicinity across the $200 \times 200 \mu\text{m}^2$ sampling grid. In Fig. 7, the collected spectra for the two sites are aligned vertically with binding energy range (eV) and dashed lines fixed to the expected position for several peaks characteristic of Ge core-level photoelectrons (3d) and Auger electron transitions ($L_3M_{45}M_{45}$, $L_2M_{45}M_{45}$). Based on the presence of these peaks and the XPS sensitivity to approximately 0.1% Ge, no Ge was found to be redeposited on the surface of the Si. This observation can be attributed to the Nova tool architecture, which confines the sputter action within the analysis area.

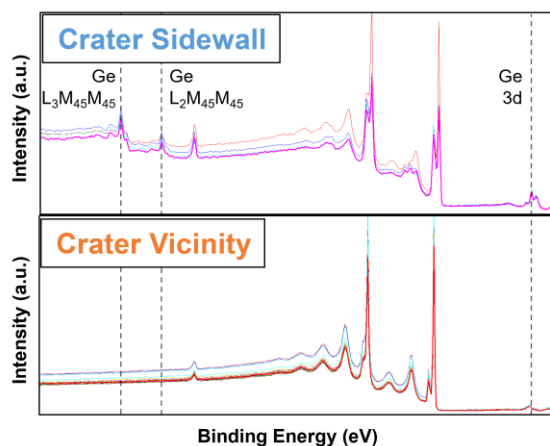


Figure 7. XPS spectra for surface scans performed along the crater sidewall (top spectra) and the crater vicinity (bottom spectra).

For tests conducted with AFM (Table 1), the measured roughness, RMS, was compared for both the crater bottom and crater vicinity to the roughness measured for the reference site 20 mm away from the crater. Recalling the subject on the Gaussian nature of the primary beam discussed in Section 3.2, there is also a change in material color contrast on the outside perimeter of the raster area (described as a halo) which is attributed to energetic neutrals that cannot be steered due to lack of charge. This was previously described as the region to be within 2 mm of the crater, where the roughness is not expected to show damage during sputtering measurements.¹⁶ First, the measured roughness for the crater bottom increased

as the primary impact energy increased. This is an expected outcome considering how the induced topography change to the floor bottom is associated with difference in erosion rate and the growth of ridge lines (ripples) as greater depths are excavated.²⁴ The roughness measured on the crater vicinity sites were comparable to the reference roughness based on relative change for each primary impact energy, supporting evidence that there was no damage to these sites around the crater.

Table 1. AFM roughness data comparing roughness, RMS (nm), for each site with respect to primary impact energy (A < B < C).

Primary Impact Energy	Mean RMS (nm)		
	Crater Bottom	Crater Vicinity	Reference
Energy A	6.9	4.0	4.7
Energy B	7.7	4.3	4.1
Energy C	8.7	3.8	4.5

3.3 Device Impact Evaluation

A desirable capability for inline SIMS metrology is to directly measure fully integrated structures, requiring the extension of the 1D depth profiling capability to 3D characterization validated downstream with electrical tests and corroborated with inline metrology (i.e. XRD, OCD) for hybrid metrology approach.^{1,15} This effort, however, could be consequential to the device quality if depth profiling comes at the cost of compromising the production wafer.

As described in Section 2.3, scribe-line measurements were performed after selected FEOL process steps of the test pFET vehicle. The wafers were then processed through the MOL and BEOL modules, followed by inline electrical tests after the first metal layer (M1) where each die is tested for reliability and functionality at specific sites that must be within acceptable limits prior to assembly. The focus here is to identify which step would be considered most detrimental to perform SIMS measurements, as well as understand the extent to which sputtering could adversely affect electrical test results. The working hypothesis for this failure mode is that particles at the atomic level would potentially land and stick to active regions of the transistor structure, thereby creating defects and negatively impact device performance and reliability.

For device reliability results, all wafers tested in each scenario achieved 100% yield for tested dies. Negative bias temperature instability (NBTI) is a reliability metric based on threshold voltage degradation generally used to quantify when a device will reach its projected end-of-life (EOL). In Fig. 8, this reliability parameter is compared across all tested scenarios, where results showed that all values acquired fall within the expected range set by the reference wafers. Based on these results, there was no observed impact to device reliability by inline SIMS sputtering.

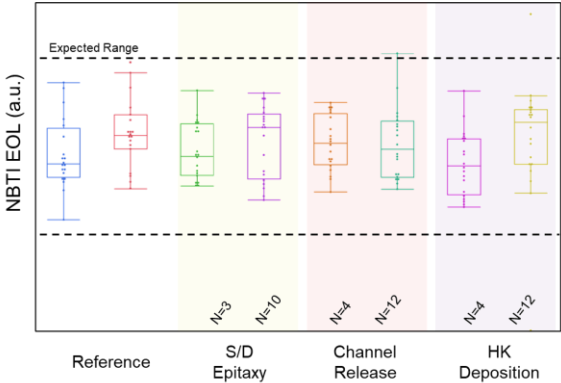


Figure 8. Post M1 device reliability results.

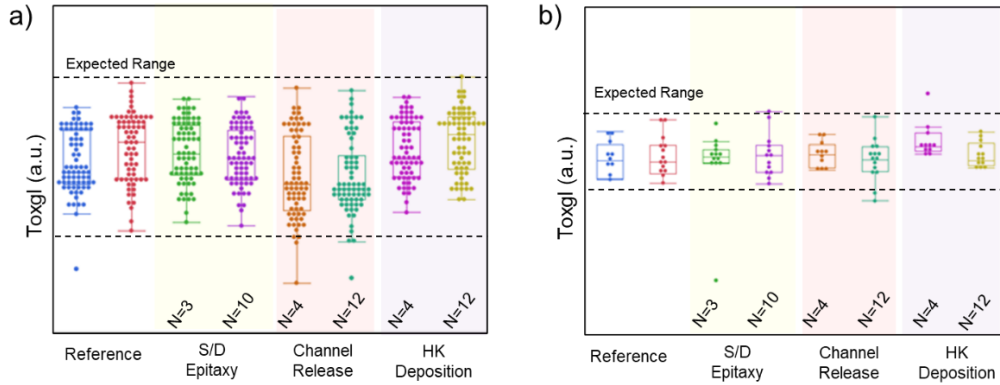


Figure 9. Post M1 electrical performance results for a) nanosheet and b) large planar devices.

Amongst a diverse set of inline test parameters acquired for each device, the selected parameter was Toxgl. This is generally considered an important device performance metric since effective gate oxide thickness is inversely proportional to the current flow, which would be susceptible to drifts in threshold voltage for such contamination in the channel region. Importantly, potential sputter contamination may occur at critical steps of the GAA device fabrication such as channel release and HK deposition; variation in these respective steps would have a great risk to performance due to the exposed nanosheet channels after removal of the sacrificial SiGe layers.¹² In Figs. 9a and 9b, the Toxgl test parameter is compared across all tested scenarios for both nanosheet devices and large planar devices, respectively. In both cases, the majority of data points were within the expected range and indicate that ion sputtering had no influence to device performance.

Data points outside of the lower expected range for both channel release wafers were further examined by performing failure analysis on select devices by looking for abnormalities to the nanosheet structure and distribution of elements using advanced TEM analysis coupled with spectroscopy methods (Fig. 10). The N=4 wafer lamella cut was analyzed for boron elemental mapping with electron energy loss spectroscopy (EELS) (Fig. 10b) and the N=12 wafer was analyzed for all other expected elements and distributions using energy-dispersive X-ray spectroscopy (EDS) (Fig. 10d). Inspection with TEM showed that the nanosheet structures were both intact, indicating changes to this active region were at the sub-nm scale and not susceptible to impact by ion sputtering. The EELS map tracing boron species in Fig. 10b showed that there was no boron contaminant detected in the structure. In addition, the EDS map in Fig. 10d further confirmed the intact structure for all elemental distributions to be as expected.

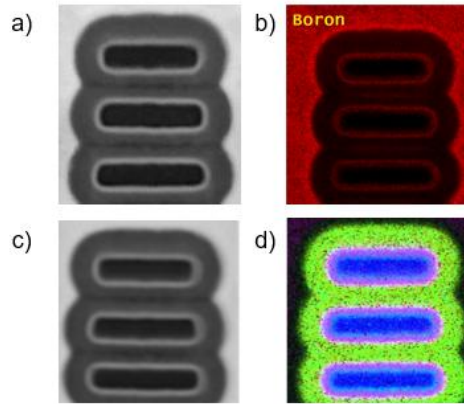


Figure 10. Post M1 failure analysis results for production wafers with tested devices yielding relatively low Toxgl values, including channel release N=4 a) cross-section TEM and b) Boron EELS map and channel release N=12 c) cross-section TEM and d) multi-element EDS map.

In conclusion to this study, performance impact was not observed for both nanosheet and even planar devices bearing larger surface area that would be more prone to sputter contamination by the inline SIMS tool. There were no trends that

distinguished impact from high SIMS dosage to low dosage, which are strong supporting points to further enable depth profiling on production wafers. It is important to note that the tests performed here were designed to represent worst case scenarios and utilization of such toolset requires careful understanding of the measurement nature upon integrating in the production environment. Overall, these results further qualify the tool design for inline SIMS as optimal for inline metrology and validate the shared technological advancement between the semiconductor industry and the SIMS community.

4. CONCLUSIONS

The Nova Metrion inline SIMS tool was evaluated for its ability to process and return the same 300mm wafer to production without compromising device performance. The tool architecture was designed and optimized to mitigate wafer contamination in the analysis chamber, therefore requiring assessments to further qualify the tool based on failure modes attributed to the crater and ion sputtering. Evidence collected here showcased qualifying attributes including acceptable crater geometry and floor topography enabling planarization, along with undamaged production wafers after ion sputtering based on surface analysis, in-line electrical tests and failure analysis verifying contamination-free nanosheet transistor devices. Prospective efforts to sputter and profile device structures for direct process feedback by inline SIMS can be carried out with high confidence and careful consideration of the nature of the measurement.

ACKNOWLEDGEMENTS

The authors would like to thank Roger Cornell, Huimei Zhou, Nicholas Latham, Christopher Carr, Nick Kochersperger, Jennifer Fullam, Johnpeter Ngunjiri, Wayne Zhao, and Luciana Meli for support of this work.

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